

Student Training Manual FOR

CYBER Fixed Module Drive Subsystem Fault Isolation

Volume 1

An Individualized Course

[illegible]

Attn: ES Information Services, STP104
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INTRODUCTION

Control Data's CYBER Fixed Module Drive (FMD) Subsystem is the latest disk storage hardware for the CDC CYBER 17X, CDC CYBER 7X and 6000 series computers. The CDC CYBER FMD, called the 885, is a 519 megabytes-per-spindle, random access disk device in which the magnetic head/disk assembly (HDA) is fixed so that only service personnel can replace them. The FMD controller, called the 7155, is a micro processor design. In addition to the 885 FMD, the controller allows, via options, attachment of 844-4X devices and up to four PP channel connections.

This course provides overall concepts of the FMD subsystem on a block diagram level. You will learn the location and purpose of major FMD and controller components and how the FMD disk pack is organized. In addition, you will learn how the logic of the FMD and controller is organized through block diagrams and simplified power supply diagrams.

You will learn the subsystem diagnostics hierarchy. You will run and interpret the diagnostics to isolate failing components. The over-all goal of the course is to provide you with the ability to use information from the diagnostics and the subsystem troubleshooting guide to replace failing components. This course does not teach logic diagram analysis.

This PLM course includes an individualized, self-study package that allows you to learn at your own pace and a laboratory module that requires an instructor and lab equipment. The multimedia lessons use audiotape, microfiche, reading assignments, review exercises, and a PLATO troubleshooting simulator to provide you with an effective learning experience. Approximately 16 hours should be allowed for the laboratory module. Contact your course administrator to schedule the lab.

Before you begin the course, check this course package to make sure it contains the following items.

- Student manual containing modules 1 through 8 and appendixes A through D.
- Six audiotapes entitled FMD Subsystem, FMD Components, HDA Components, Detailed Block Diagram, Basic Power Sequence, and 7155 Block Diagram.
- Three ESE microfiche entitled FMD Subsystem, FMD Components, and HDA Components.

CYBER Fixed Module Drive Introduction

The following manuals are necessary for the reference reading assignments and must be available while you are taking this course.

<u>Title</u>	<u>Publication Number</u>
FMD Controller Manual	GF60455690
BZ703 CYBER Disk Storage Theory of Operation Manual	83322880
BZ703 CYBER Disk Storage Manual, Volume 1	GF83322860
7155 Troubleshooting Guide (trade secret proprietary)	60456010
Operator Troubleshooting/Maintenance Guide	60456650
Malet Documentation Microfiche	53140094
7155 Disk Storage Subsystem General Description Manual	60455860

If this is your first experience with PLATO assisted learning, read appendix A, Using Individualized Instruction, before you sign on to the terminal. this appendix explains the basic philosophy and organization of self-study courses. Appendix B explains the correct procedure for signing on to the PLATO terminal. Appendix C describes the use of microfiche. Appendix D contains the text of the audiotapes in this package.

Begin the course by reading module 1.

MODULE 1

INTRODUCTION TO THE FMD SUBSYSTEM

This module will acquaint you with the major components of the FMD subsystem. You will learn how the elements of the controller and unit are organized through block diagrams.

PRETEST

To begin this module, sign on to the PLATO terminal and read the objectives. If you feel you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLM will assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test, ask for an assignment.

LEARNING ACTIVITIES

In the Assigned column below, place a checkmark by each activity assigned to you by PLM. Then proceed through those assigned activities. Check off each activity as you complete it. You may choose to do all of the activities or do some activities more than once.

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	1-A	Audio/Microfiche: FMD Subsystem. This activity describes the fixed module drive subsystem configurations, options, and block diagram elements.	1-3
_____	_____	1-B	Reference Reading: General Description. This activity describes the hardware elements, configurations, storage theory, and specifications for the fixed module drive subsystem.	1-4

CYBER Fixed Module Drive
Module 1

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	1-C	Exercise: Subsystem Review. This activity reinforces learning activities 1-A and 1-B.	1-5

LEARNING ACTIVITY 1-A. AUDIO/MICROFICHE: FMD SUBSYSTEM

This activity describes the FMD subsystem configurations, options, and block diagram elements.

OBJECTIVE

- You will be able to identify the major fixed module drive subsystem block diagram components and describe the function of each.

To begin the activity, load microfiche FMD Subsystem (75445260) into your projector and audiotape FMD Subsystem (75445259) into your cassette player and proceed through the activity.

STUDENT NOTES

CYBER Fixed Module Drive
Learning Activity 1-B

LEARNING ACTIVITY 1-B. REFERENCE READING: GENERAL DESCRIPTION

This activity describes the hardware elements, configurations, storage theory, and specifications for the FMD subsystem.

OBJECTIVES

- You will be able to identify the major fixed module drive subsystem block diagram components and describe the function of each.

Read section 1 in the 7155 Disk Storage Subsystem General Description Manual, publication number 60455860.

NOTE: This course is based on the 7155-1 (FA211-A) controller.

ST 10397-1 ADDS PP ACCESS up to 4
10398-1 ADDS 844 drives 1-8
10399-1 2 to 8 885 drives
844 885
322 12bit words per sector 322
24 sectors per track 32
19 tracks per cylinder 40
823 cylinders pack 843

LEARNING ACTIVITY 1-C. EXERCISE: SUBSYSTEM REVIEW

This activity reviews the FMD subsystem components.

OBJECTIVE

- You will be able to identify the major fixed module drive subsystem block diagram components and describe the function of each.

After completing the exercise, check your answers with those given at the end of this learning activity.

Directions: Each of the following statements is followed by four answers. Read each statement and fill in the blank with the letter of the answer that most correctly completes that statement.

1. The element of the 7155 controller that stores the MA721 controlware is the_____.
 - a. Processor channels
 - ☒ b. Processor memory
 - c. ECC control
 - d. Access control
2. The ECC control element of the 7155 controller generates _____.
 - ☒ a. CRC patterns
 - b. Address fields
 - c. Unit addresses
 - d. Controlware
3. The_____executes MA721 controlware in the 7155 controller.
 - a. Data format ECC control
 - ☒ b. Processor
 - c. Processor memory
 - d. Processor channels

CYBER Fixed Module Drive
Learning Activity 1-C

4. The 885 drive interface provides a connection between the _____ and the 885 drives in the 7155 controller.
- a. 844 drive
 - b. PP access
 - c. Processor channels
 - ☒ d. Data format/ECC control
5. The access control element determines the _____ to be connected in the 7155 controller.
- a. 844 drive
 - b. 885 drive
 - ☒ c. P-P access
 - d. Processor channel
6. The track on a disk pack is divided into _____.
- a. Positions
 - b. Heads
 - ☒ c. Sectors
 - d. Cylinders
7. The 7155-1 controller option that expands the 885 drive interface for eight additional drives is the _____.
- ☒ a. 10399-1.
 - b. FA211.
 - c. BZ703.
 - d. 10397-1.
8. The drives _____ element converts data to write current.
- a. Head positioner
 - ☒ b. Read/write electronics
 - c. Head assembly
 - d. Disk pack

Directions: After reading each of the following statements, fill in the blank(s) with a word or words to complete the statement and make it true.

9. The process of loading controlware in to the 7155 controllers memory is called a autoload operation.
10. Standard option 10397-1 adds 1 PP access to the 7155-1 controller.

CYBER Fixed Module Drive
Learning Activity 1-C

11. The equipment number for the 7155 controller is FA 211.
12. The 7155 controller, with options, can interface with a maximum of 4 PP channels.
13. Standard option 10399-1 expands the 7155-1 controller drive interface to allow a maximum of 8 additional 885 devices.
14. With all options, a 7155 controller could have a maximum of 16 885 devices, 8 844 drives, and 4 PP accesses.
15. The smallest addressable area on a disk pack is called a sector.
16. The element of the disk drive that moves the head assembly is called the positioner.
17. The maximum number of controller channel interfaces on a 885 device is two.
18. The element of a disk drive that determines which controller channel interface is connected is the select/reserve logic.
19. The disk pack is rotated by the drive motor.
20. The data field of a sector contains 322 12-bit words.
21. One 885 cabinet has 2 devices.
22. The amount of recording surface available under one head, without moving the heads, (a stopping position) is a definition of a track.
23. The equipment number for the 885 is BZ703.
24. The disk pack on the 885 is not removed by an operator.
25. The program that the processor of the 7155 executes is called Control Room.
26. The unit address of the disk drive is determined by the controller port where the interface cable is connected.

CYBER Fixed Module Drive
Learning Activity 1-C

ANSWERS to LEARNING ACTIVITY 1-C

Correct your answers.

- | | |
|--------------|-------------------------|
| 1. b | 14. 16, 8, 4 |
| 2. a | 15. sector |
| 3. b | 16. positioner |
| 4. d | 17. two |
| 5. c | 18. select/reserve |
| 6. c | 19. rotated |
| 7. a | 20. 322 |
| 8. b | 21. two |
| 9. auto load | 22. track |
| 10. one | 23. 885 or FMD |
| 11. FA211 | 24. 885 or FMD or BZ703 |
| 12. four | 25. MA721 controlware |
| 13. eight | 26. unit or device |

CYBER Fixed Module Drive
Learning Activity 1-C

POST TEST

When you have completed the learning activities assigned for module 1, sign on to the PLATO terminal and take the module 1 test.

You may use your student manual and your reference manuals during the test. Be sure to take them with you to the PLATO terminal.

Depending on the results of the test, you will be told to review some of the activities in this module or to go on to module 2.

MODULE 2

FIXED MODULE DRIVE COMPONENTS

This module will acquaint you with the major components of the FMD unit. You will learn the location and function of the components through locator diagrams.

PRETEST

To begin this module, sign on to the PLATO terminal and read the objectives. If you feel you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLATO learning management (PLM) will assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test, ask for an assignment.

LEARNING ACTIVITIES

In the Assigned column below, put a checkmark by each activity assigned to you by PLM. Study the assigned activities and check off each activity as you complete it. You may choose to do all of the activities or some activities more than once.

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	2-A	Audio/Microfiche: FMD Components. This activity describes the function of the major components of the 885 Fixed Module Drive.	2-3
_____	_____	2-B	Audio/Microfiche: HDA Components. This activity describes the components of the head disk assembly (HDA) and logic chassis of the 885 Fixed Module Drive.	2-4

CYBER Fixed Module Drive
Module 2

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	2-C	Reference Reading: Component Descriptions. This activity describes the features, specifications, physical and functional elements, and operation for the fixed module drive components.	2-5
_____	_____	2-D	Exercise: FMD Components Review. This activity reinforces the information about the fixed module drive components in learning activities 2-A, 2-B, and 2-C.	2-6

LEARNING ACTIVITY 2-A. AUDIO/MICROFICHE: FMD COMPONENTS

This activity describes the function of the major components of the 885 Fixed Module Drive.

OBJECTIVE

- You will be able to describe the function of the major components of the 885 Fixed Module Drive.

Load microfiche FMD Components (75445264) into your projector and audiotape FMD Components (75445263) into your cassette player and proceed with the activity.

STUDENT NOTES

CYBER Fixed Module Drive
Learning Activity 2-B

LEARNING ACTIVITY 2-B. AUDIO/MICROFICHE: HDA COMPONENTS

This activity describes the components of the head disk assembly (HDA) and logic chassis of the 885 Fixed Module Drive.

OBJECTIVE

- You will be able to describe the components of the HDA and logic chassis of the 885 Fixed Module Drive.

Load microfiche HDA Components (75445266) into your projector and audiotape HDA Components (75445265) into your cassette player and proceed with the activity.

STUDENT NOTES

LEARNING ACTIVITY 2-C. REFERENCE READING: COMPONENT DESCRIPTIONS

This activity describes the features, specifications, physical and functional elements, and operations for the fixed module drive components.

OBJECTIVE

- You will be able to describe the function of the major components of the 885 Fixed Module Drive.

Read section 1, section 2, and the paragraphs on ventilation, cooling, and disk rotation in section 3 of the CYBER Disk Storage BZ703 General Description Theory of Operation Manual, publication number 83322880.

Read sections 1, 2A, and 2B in the CYBER Disk Storage BZ703 (Volume 1) Manual, publication number GF83322860.

CYBER Fixed Module Drive
Learning Activity 2-D

LEARNING ACTIVITY 2-D. EXERCISE: FMD COMPONENTS REVIEW

This activity reviews the fixed module drive components. After completing the exercise, check your answers with those given at the end of this learning activity.

OBJECTIVE

- You will be able to describe the function of the major components of the 885 Fixed Module Drive.

Directions: After reading each of the following statements, fill in the blank(s) with a word(s) to complete the statement and make it true. You may refer to the chassis map in figure 2-1 at the end of the questions.

1. The high pressure blower supplies air to the HDA.
2. Switches located in the HDA input ports monitor the air flow in the HDAs.
3. The low pressure blower supplies air to the logic chassis and DC power supplies.
4. The air from the high pressure blower passes through the absolute filter then to the HDAs.
5. The device DC power switch is located on the A 4 power panel.
6. The center position of the device DC power switch applies DC power to both.
7. The physical locator code for the front portion of the DC power supply is A 3.
8. The power requirements for the FMD are 50/60 Hz and 400 Hz.
9. The 50-Hz drive motor circuit breakers are located on the AC supply.

CYBER Fixed Module Drive
Learning Activity 2-D

10. The physical locator codes for the AC power supply are A2 and A11.
11. The A9 physical locator code specifies the maintenance.
12. The switch/indicator on the operator panel that informs the operator that no write operation can take place is labeled read only.
13. To power up the FMD independent of the controller, the local/remote switch must be in the local position.
14. The CE rezero switch is enabled by the maintenance switch.
15. The drive motor is connected to the HDA by a belt.
16. On a power off, the brake stops the HDA within 20 seconds.
17. The HDA has 20 data surfaces and one servo surface.
18. One data head arm assembly has 4 heads.
19. There is one servo head and 40 moveable data heads.
20. The type of logic board at location 07 is JCX.

Directions: Write your answer in the space following each question.

21. Where is the thermostat that senses the logic chassis temperature located?

top of logic chassis

22. What are the names of the eight light emitting diodes (LED) on the unit power sequence board?

B start
B stop
B air ok
A start
A stop
A air ok
Frame chkd.
Frame sequence

CYBER Fixed Module Drive
Learning Activity 2-D

23. How many controller interface cables are necessary for one device channel?

/

24. Where is the 60-Hz, drive motor, thermal reset button located?

bottom of motor

25. What is the function of the logic board at location 21?

I/O buffer

26. What is the name of the switches on the logic board at location 20?

unique I/O switches

CYBER Fixed Module Drive Learning Activity 2-D

DEVICE A		
40	WRITE PLO	-DMX
39	QUADBIT SERVO DECODER	-FYX
38	INDEX/SERVO	-FZX
37	VELOCITY GEN & LEVEL DETECT	-GKX
36	DESIRED VELOCITY	-GJX
35	MODE SELECT	-GLX
34	SERVO CONTROL NO. 2	-FMX
33	SERVO CONTROL NO. 1	-FLX
32	HDA SEQUENCING NO. 2	-HBX
31	HDA SEQUENCING NO. 1	-HFX
30		
29		
28	TARGET REGISTER	-HAX
27	MULTIPLEXER NO. 3	-GZX
26	MULTIPLEXER NO. 2	-GZX
25	MULTIPLEXER NO. 1	-GZX
24	READ/WRITE CONTROL	-HMX
23	INTERFACE CONTROL	-HEX
22	INTERFACE DECODE	-GYX
21	I/O BUFFER	-HDX
20	DUAL CHANNEL LOGIC	-HLX
19		
18		
17		
16	HD SELECT/DIFF/CAR #2	-HGX
15	HAR AND DIFF COUNTER	-HCX
14		
13		
12		
11	READ DATA SEPARATOR AND MASTER PLO	-FSX
10	HIGH RESOLUTION READ DECODER	-GTX
09	LOW RESOLUTION READ DECODER	-JDX
08		
07	WRITE COMPENSATION	-JCX
06		
05		
04	CHAN II XMTRS/RCVRS - BIDIRECTIONAL	-HJX
03	CHAN I & II XMTRS/RCVRS - UNIDIRECTIONAL	-HKX
02	CHAN I XMTRS/RCVRS - BIDIRECTIONAL	-HJX
01		

DEVICE UNIQUE I.D.

NOTE:

1. CARD TYPE IS FOUR CHARACTERS. FIRST CHARACTER (NOT SHOWN) INDICATES CARD REVISION. IT MAY BE EITHER A NUMBER OR LETTER. REFER TO SPARE PART LIST IN MAINTENANCE MANUAL VOL I FOR APPLICABLE CARD TYPE AND PART NUMBER.
2. DEVICE B IDENTICAL TO DEVICE A.

Figure 2-1. 885 Chassis Map

CYBER Fixed Module Drive
Learning Activity 2-D

ANSWERS TO LEARNING ACTIVITY 2-D

Correct your answers.

- | | |
|-------------------------|--|
| 1. high | 17. twenty, twenty-one if the HDA has the fixed head feature |
| 2. air pressure or flow | 18. four |
| 3. DC power supply | 19. forty |
| 4. absolute | 20. -JCX |
| 5. DC power supply | 21. above the logic chassis |
| 6. both devices | 22. Start B, stop B, air OK B, start A, stop A, air OK A, frame check, and frame sequence. |
| 7. A3 | 23. one |
| 8. 400 | 24. on the bottom of the motor |
| 9. AC power supply | 25. I/O buffer |
| 10. A17 | 26. Unique ID switches |
| 11. maintenance panel | |
| 12. operator, read only | |
| 13. local | |
| 14. system maintenance | |
| 15. belt | |
| 16. twenty | |

POST TEST

When you have completed the learning activities assigned for module 2, sign on to the PLATO terminal and take the module 2 test.

You may use your student manual and your reference manuals during the test. Be sure to take them with you to the PLATO terminal.

Depending on the results of the test, you will be told to review some of the activities in this module or to go on to module 3.

MODULE 3

INTRODUCTION TO THE FMD THEORY

This module will acquaint you with the FMD unit theory. You will learn how the FMD pack is organized and the elements of the servo disk. You will learn how the logic is organized through block diagrams and follow a basic power-up sequence.

PRETEST

To begin this module, sign on to the PLATO terminal and read the objectives. If you feel you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLM will assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test, ask for an assignment.

LEARNING ACTIVITIES

In the Assigned column below, put a checkmark by each activity assigned to you by PLM. Proceed through the assigned activities and check off each activity as you complete it. You may choose to do all of the activities or do some activities more than once.

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	3-A	Text Reading: Pack Organization. This activity describes the major organizational areas of the 885 Fixed Module Drive disk pack.	3-5
_____	_____	3-B	Exercise: Pack Organization Review. This activity reinforces learning activity 3-A.	3-19

CYBER Fixed Module Drive
Module 3

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	3-C	Text Reading: Servo Disk Elements. This activity describes the elements of the servo disk, servo pulses, servo bytes, index, servo zones, and servo-to-data surface correlation.	3-23
_____	_____	3-D	Reference Reading: Servo Disk. This activity describes the elements of the servo disk, servo bands and bytes, servo zones, and servo to data surface correlation.	3-34
_____	_____	3-E	Exercise: Servo Disk Elements Review. This activity reinforces learning activities 3-C and 3-D.	3-35
_____	_____	3-F	Text Reading: Functional Diagrams. This activity describes the functional areas of the FMD basic and unit functional block diagrams.	3-39
_____	_____	3-G	Exercise: Functional Diagrams Review. This activity reinforces learning activity 3-F.	3-44
_____	_____	3-H	Text Reading: I/O Commands. This activity describes the control and status commands and the purpose of each interface signal.	3-47
_____	_____	3-I	Reference Reading: Commands and Signals. This activity lists and describes all 4X and 8X commands and all controller/device signal lines.	3-51

CYBER Fixed Module Drive
Module 3

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	3-J	Exercise: I/O Commands Review. This activity reinforces learning activities 3-H and 3-I.	3-52
✓ _____	_____	3-K	Audiotape: Detailed Block Diagram. This activity describes the detailed block diagram of the FMD logic.	3-55
✓ _____	_____	3-L	Exercise: Detailed Block Diagram Review. This activity reinforces learning activity 3-K.	3-63
✓ _____	_____	3-M	Audiotape: Basic Power Sequence. This activity describes the basic power sequence diagrams of the FMD power supply.	3-69
✓ _____	_____	3-N	Exercise: Basic Power Sequence Review. This activity reinforces learning activity 3-M.	3-77

LEARNING ACTIVITY 3-A. TEXT READING: PACK ORGANIZATION

This activity describes the major organizational areas of the 885 Fixed Module Drive disk pack.

OBJECTIVE

- You will be able to list the major organizational areas of the 885 Fixed Module Drive and describe the function of each.

The purpose of the FMD disk pack is to store data. The surface of the disk is coated with magnetic oxide. Data is transferred to and from the disk surface by a read/write head using a magnetic recording technique called modified frequency modulation (MFM). The MFM method is used to transfer data at the rate of 9.584 MHz. This rate of transfer makes the cell time, or time to write or read a binary bit, approximately 100 nanoseconds (ns).

The 885 Fixed Module Drive disk pack is enclosed in a plastic shroud along with the recording heads. It's called an HDA (see figure 3-1). The HDA is not removeable by the site operator, hence the name fixed module.

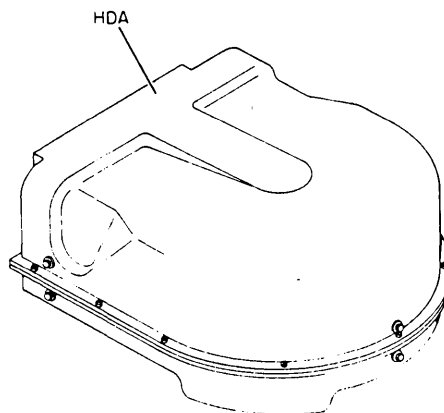


Figure 3-1. HDA

CYBER Fixed Module Drive
Learning Activity 3-A

The HDA, like most Control Data disk packs, is organized into cylinders, tracks and sectors. A cylinder is the recording surface beneath all heads at a stopping position. A track is the recording surface beneath one head at a stopping position. A sector is a division of a track and the smallest addressable area on a disk pack. (see figure 3-2)

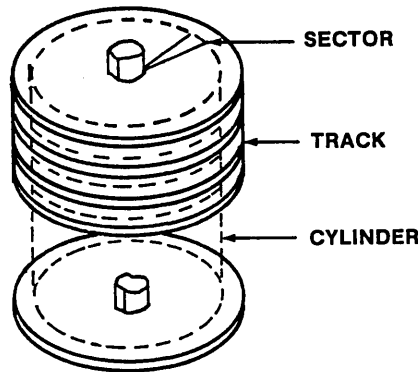


Figure 3-2. Data Organization

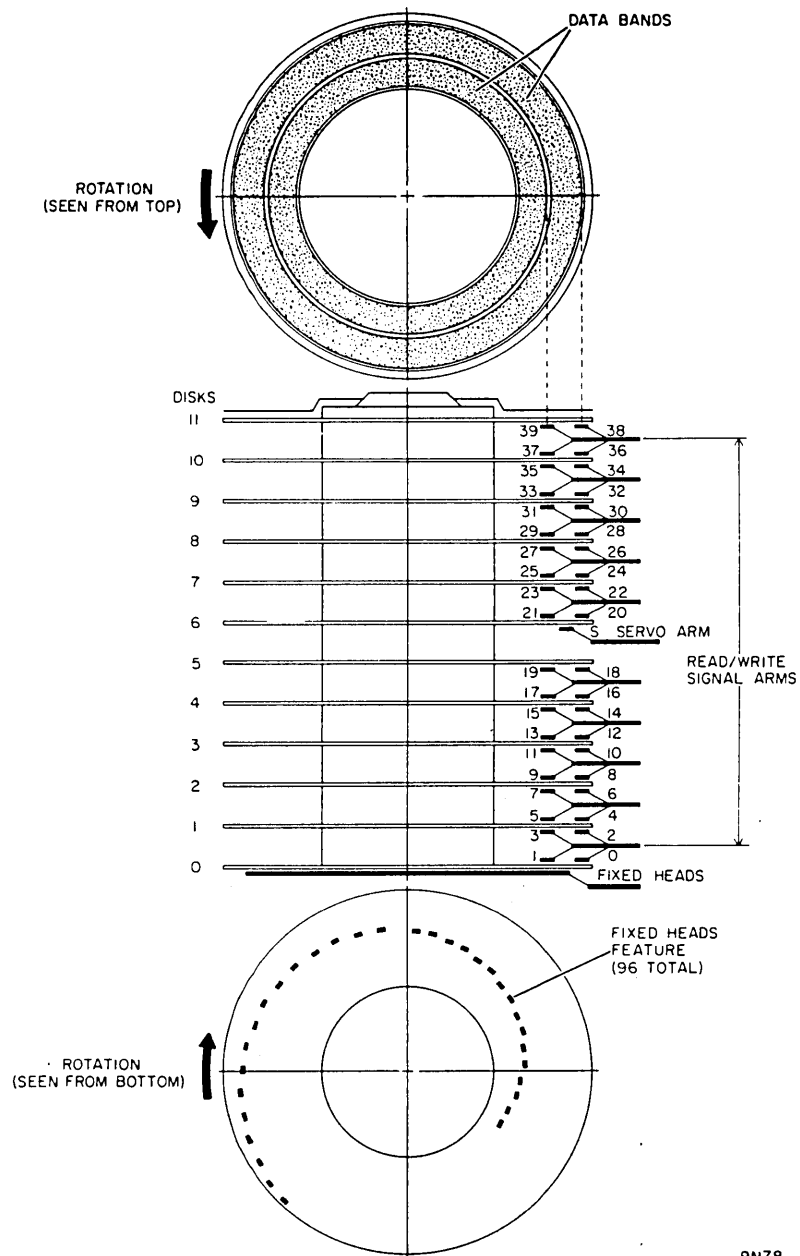
The HDA contains 12 magnet recording disks, 40 moveable read/write heads, and 1 servo head (see figure 3-3). The heads are mounted on arms attached to a positioning mechanism called a carriage. There are two read/write heads for each of 20 disk surfaces. There are four read/write heads on each data head arm assembly: two upper heads and two lower heads.

The servo head can stop at 844 positions. The outermost stopping position is position zero. The position closest to the center of the disk is position 843.

The two read/write heads for each data surface are stacked vertically and positioned simultaneously with the servo head. Each stopping position of the servo head defines two tracks on each data disk surface.

When the servo head is positioned to one specific track, the read/write heads are positioned to 40 tracks.

CYBER Fixed Module Drive
Learning Activity 3-A



9N78

Figure 3-3. HDA Heads and Disks

CYBER Fixed Module Drive
Learning Activity 3-A

Each read/write head has its own data band of 844 tracks. The data tracks for one head do not overlap the data tracks of the other head. As an option, the HDA may have the fixed head feature. The fixed heads are located on the bottom surface of the bottom disk in the HDA. The heads are called fixed because they are not attached to the moveable carriage. There are 96 fixed heads, so there are 96 tracks on the fixed head disk surface. An HDA cylinder is the recording surface beneath all 40 recording heads. There are 844 stopping positions so the FMD has 844 cylinders.

Forty recording heads and 844 cylinders make a total of 33,760 tracks for the HDA. If the fixed head feature is present, there will be 96 additional tracks.

All tracks are divided into sectors, and all the sectors are the same size (see figure 3-4). That is, the physical size of a sector in an outside track is larger than the physical size of a sector in an inside track. However, each contains the same number of bits. The bits are packed a little closer together on the inner tracks. The inner tracks have higher bit density than the outer tracks.

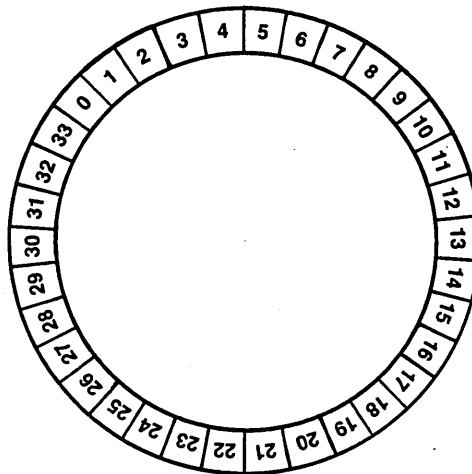


Figure 3-4. Physical Sectors

CYBER Fixed Module Drive
Learning Activity 3-A

An FMD track is divided into 34 sectors, numbered 0 through 33. Due to imperfections in the magnetic oxide coating of the disk surface, some areas may not retain the data. These imperfections are called bad spots, defects, or flaws. A flaw makes a sector unuseable for recording data. Since it is normal to have some flaws, the FMD subsystem expects 32 of the 34 physical sectors in a track to be free of flaws. If more than two sectors are flawed, then the entire track can't be used.

The term physical sector is used to indicate all the sectors. The term logical sector specifies the 32 sectors that must be free of flaws.

When there are no flaws, the first 32 physical sectors are also the 32 logical sectors. The last two physical sectors are not used (see figure 3-5).

NO FLAWS

LOGICAL	23	24	25	26	27	28	29	30	31				33
PHYSICAL	23	24	25	26	27	28	29	30	31	32	33		33

Figure 3-5. Sector Numbering With No Flaws

When there is one flaw, the sector that has the flaw is skipped in the logical sector numbering. The last physical sector is not used. In figure 3-6, physical sector 30 is flawed so physical sector 31 becomes logical sector 30 and physical sector 32 becomes logical sector 31.

ONE FLAW

LOGICAL	23	24	25	26	27	28	29	X	30	31			33
PHYSICAL	23	24	25	26	27	28	29	30	31	32	33		33

Figure 3-6. Sector Numbering With One Flaw

CYBER Fixed Module Drive
Learning Activity 3-A

When there are two flaws, the sectors that have flaws are skipped in the logical sector numbering. In figure 3-7, physical sectors 29 and 31 are flawed so physical sector 30 becomes logical sector 29 and physical sectors 32 and 33 become logical sectors 30 and 31.

TWO FLAWS												
LOGICAL	22	24	25	26	27	28	X	29	X	30	31	32
PHYSICAL	22	24	25	26	27	28	29	30	31	32	33	34

Figure 3-7. Sector Numbering With Two Flaws

Notice that the physical and logical sector numbering is the same in a track until there is a flawed sector, then the logical sector numbering skips the defective sector.

When there are more than two flawed sectors, the entire track is not useable because it doesn't have thirty-two good sectors.

Addressing is specifying which sector on the disk pack is to be used for a read or write operation. The first step is to select one of the 844 cylinders and position the heads to this cylinder. The next step is to select one of the 40 moveable heads or one of the 96 fixed heads. Now that the track is selected, one of the 32 logical sectors must be specified.

The disk is divided into sectors by the logic that generates signals called sector marks from information on the servo disk surface.

The sector mark specifies the end of one sector and the beginning of the next sector. The sector is further divided into fields as shown in figure 3-8. The number at the bottom of each area indicates the number of bits in that field.

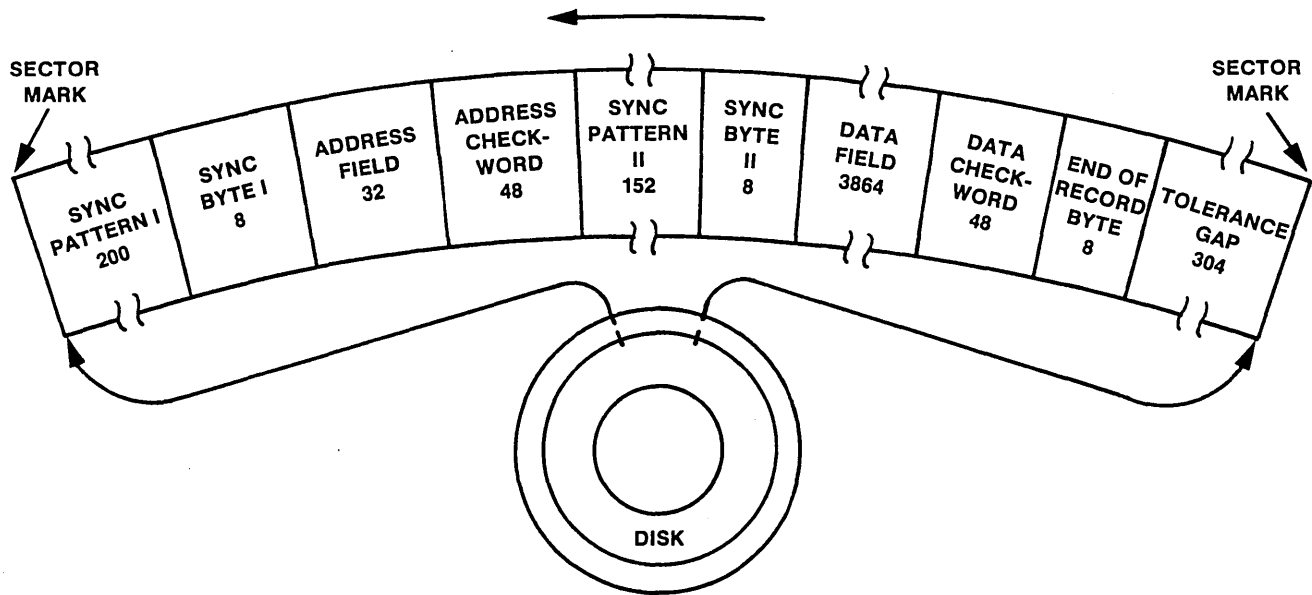


Figure 3-8. Sector Format

CYBER Fixed Module Drive
Learning Activity 3-A

Sync pattern I is a field of 200 consecutive zero bits. The field is used to synchronize the read logic to the speed of the disk pack. After the sector mark has occurred, the head is turned on to read and the data is transmitted to the read logic. The speed at which these zero bits come off the disk determines the frequency at which the logic operates to receive the information. Once the circuitry has been locked in, it changes as necessary to keep the electronics synchronized with any slight variations in the speed of the disk pack.

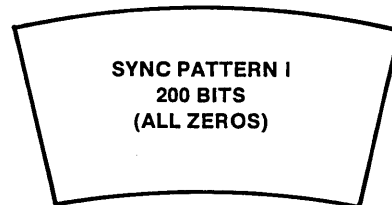


Figure 3-9. Sync Pattern I

The sync byte I is a special 8-bit byte recorded with a binary 00011001 pattern. When detected, it is used to alert the logic that the address field is about to be read (see figure 3-10).

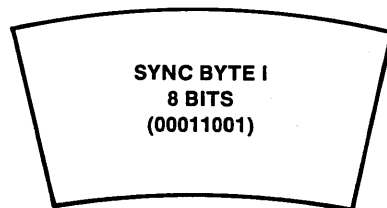


Figure 3-10. Sync Byte I

CYBER Fixed Module Drive
Learning Activity 3-A

The address field is written by the factory when the disk pack is manufactured or by qualified site personnel. The process of writing addresses is known as formatting, writing address tags, or writing headers. Under normal subsystem operation, the address field will be read only to verify that it is the correct sector for the read or write operation. This is sometimes called a verify or compare operation because the logic compares the address field on the disk with the address requested.

The address field contains the unique information that identifies the sector from all other sectors on the disk pack (see figure 3-11). Bits 0 through 7 specify one of the 32 logical sectors in a track. Bits 8 through 15 specify one of the 40 moveable heads or one of the 96 fixed heads. Bits 16 through 25 specify one of the 844 cylinders. Bits 26 through 29 are not used. Bit 30 is used to indicate a special flaw table sector. Bit 31 is set in all remaining sectors of a track that has more than two defective sectors.

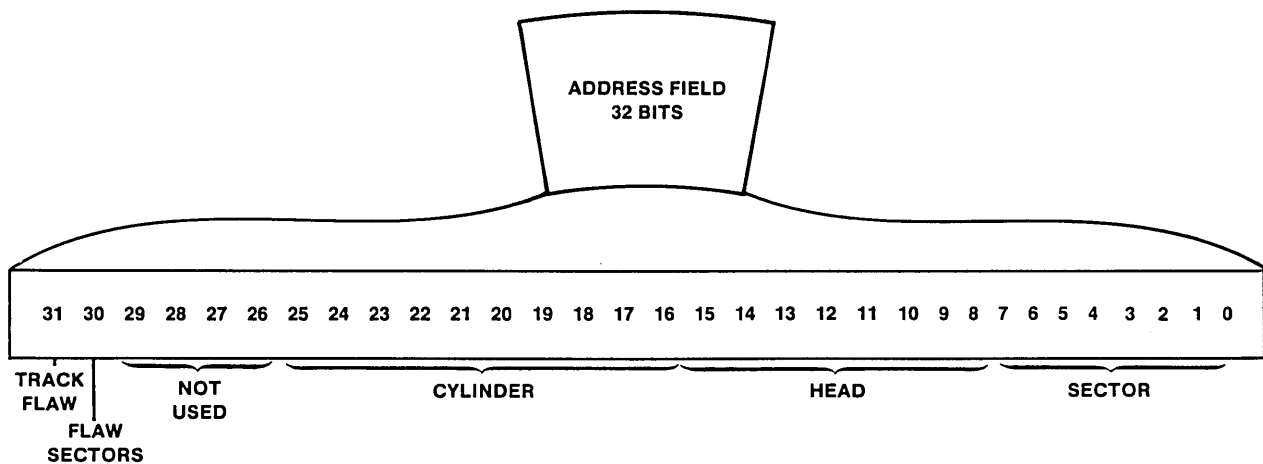


Figure 3-11. Address Field

CYBER Fixed Module Drive
Learning Activity 3-A

Each bit that was written into the address field when the addresses were written also went through a controller circuit called a checkword generator (see figure 3-12). The checkword is an error detection word. The checkword is written on the disk and will be read each time the address field is read. When reading the address, the bits that are read will again be sent to the checkword generator. After reading the checkword, the contents of the checkword generator should equal zero if no errors have occurred. If the contents of the checkword generator are nonzero, an error in reading or writing has occurred.

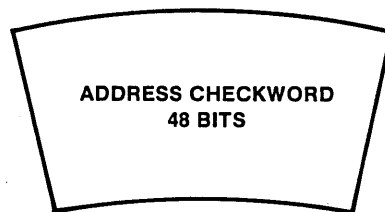


Figure 3-12. Address Checkword

The purpose of sync pattern II and sync byte II is the same for the data field as sync pattern I and sync byte I were for the address field. Note that these two fields are written every time the data field is written, while sync pattern I and sync byte I are rewritten only during pack formatting.

The data field is the area where the data words are serially recorded, bit-by-bit. When the last bit of one word is written, the first bit of the next word follows immediately, so there are no blank spaces in the data field (see figure 3-13).

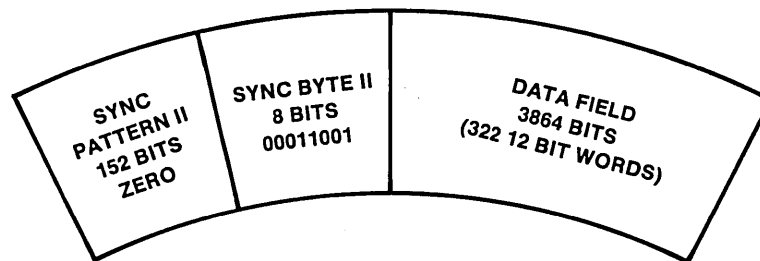


Figure 3-13. Data Field

The data checkword is written immediately after the data field. The checkword is used for detecting errors after reading the data field (see figure 3-14).

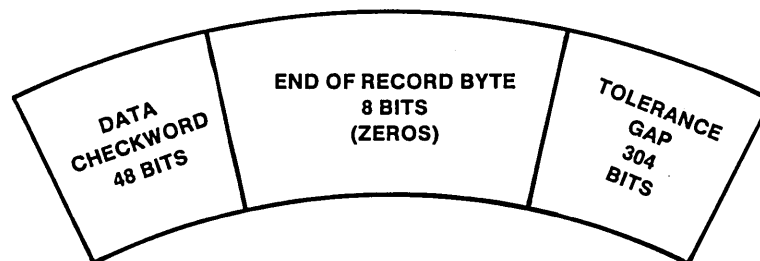


Figure 3-14. Data Checkword

CYBER Fixed Module Drive
Learning Activity 3-A

The end of record byte is written immediately after the data checkword to prevent a possible noise pulse from being written into the checkword field when the head is shut off. By writing eight zeros at the end of the checkword field and then shutting off the head, a noise spike will not cause damage to useful data.

The tolerance gap is not actually recorded. A space equivalent to 304 bits is left open to compensate for speed variations in the disk pack. As the rotational speed increases, each bit of magnetism on the surface becomes slightly longer. If no space is allowed to take up this difference, data from two sectors could overlap and make both sectors useless.

All sectors on the disk pack have the same fields arranged in exactly the same order. The sector's purpose is to provide addressable areas for recording and retrieving data.

The data fields of all sectors on cylinder 0 through cylinder 840 are available for the computer operating system to write and read data. There are some special sectors on the disk pack. The data field of the special sectors is not used by the operating system program for recording data under normal operation.

The special sectors are located on the disk pack beginning with cylinder 841 (1511 octal).

At head zero, sector zero's data field contains the pack serial number and the date the pack was manufactured. Sector 1 contains a table of defective tracks that were present when the pack was manufactured. Sectors 2 through 18 contain a table or map of sectors that were found defective at the factory (see figure 3-15).

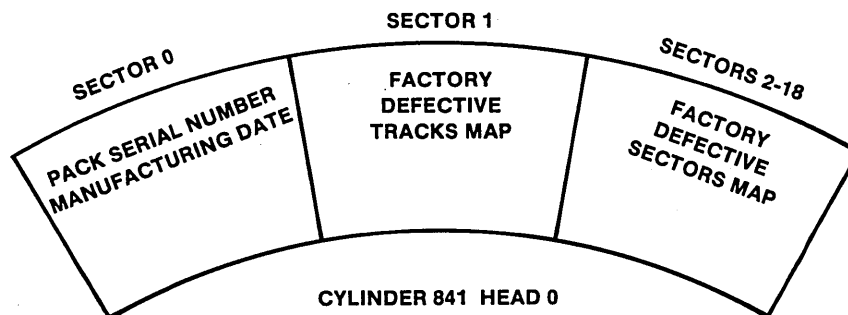


Figure 3-15. Factory Sectors

At head 1, the data fields of sectors 0 through 18 contain the utility flaw map. The factory defective track and sector information is also located there, and it is an area where additional defective tracks and sectors can be listed. During the operational life of the HDA, some previously good areas of the disk surface may lose the ability to retain data. Through a special utility program, the site personnel can rewrite the address fields of the sectors on a track to skip the defective sector(s). The defective sections are written with zeros. If more than two sectors are defective, the defective track bit will be written in the address fields of all sectors on the track. The utility program lists these new defective sectors or tracks in the utility flaw map at sectors 0 through 18 (see figure 3-16).

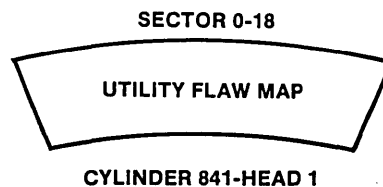


Figure 3-16. Utility Flaw Map

The operating system programs can access cylinder 841 and read sectors 0 through 18 of head 1 to obtain a complete list of the defective sectors and tracks.

CYBER Fixed Module Drive
Learning Activity 3-A

A computer system may be deadstarted from an FMD if the deadstart information has been previously recorded on the disk pack. An MSL utility program called TDX is used to place the deadstart information on the disk pack; it is stored in the data field of sector 30 head 1 (see figure 3-17).

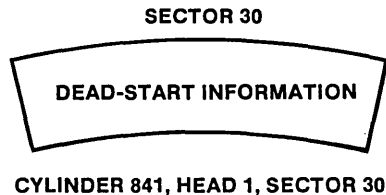


Figure 3-17. Deadstart Information

As you may recall from an earlier learning activity, the controller must have a program called controlware loaded into the processor memory to operate fully. The controlware can be loaded from the PPU or from the disk.

To load controlware from the disk, it must first be stored on the disk pack by diagnostic programs. This operation will be covered in a later learning activity. The controlware is stored at head 2 in the data fields of the sectors 1 through 30.

The remaining heads 3 through 39 and their sectors at cylinder 841 are used by diagnostic programs such as write and read tests.

All the heads and sectors at cylinder 842 (1512 octal) are also reserved for diagnostic use. Cylinder 843 (1513 octal), the innermost cylinder, is reserved for future use.

You have now completed learning activity 3-A.

LEARNING ACTIVITY 3-B. EXERCISE: PACK ORGANIZATION REVIEW

This activity reviews the fixed module drive pack organization.

OBJECTIVE

- You will be able to list the major organizational areas of the 885 Fixed Module Drive and describe the function of each.

After completing the exercise, check your answers with those given at the end of this learning activity.

Directions: After reading each of the following statements, fill in the blank(s) with a word or words to complete the statement and make it true.

1. Cell time is defined as the length of time required to write or read one data bit.
2. The FMD uses a recording technique called modified frequency modulation.
3. HDA stands for head disk assembly.
4. The recordable surface beneath all heads at a stopping position, is known as a cylinder.
5. The recordable surface beneath one head at a stopping position, is known as a track.
6. There are 4 data heads per read/write head arm assembly.
7. Each data disk surface has a total of 2 moveable read/write heads.
8. Each data disk surface has a total of 844 tracks.
9. The stopping position of the servo head closest to the center of the disk is cylinder 844.
10. The fixed head fixture adds a total of 96 heads to the bottom surface of the bottom disk in the pack.

CYBER Fixed Module Drive
Learning Activity 3-B

11. The data tracks for one moveable read/write head do not (do/do not) overlap the data tracks of the other head on the same disk surface.
12. The HDA is not (is/is not) physically removeable by the site operator.
13. The FMD track is physically divided into 34 sectors.
14. The term logical (physical/logical) sector specifies the 32 sectors that must be free of flaws for the track to be useable.
15. Physical sector 25 is flawed; physical sector 26 becomes logical sector 25.
16. When a track has more than 2 sectors that are flawed, the entire track is not useable.
17. When a track has no flaws, physical sectors 33 and 34 are not used.
18. The three selections necessary to select any address on the disk pack are the cylinder, track, and sector.
19. Bit 31 of the address field is set to specify the track is defective (more than two flawed sectors).
20. Bits 16 through 25 of the address field specify the cylinder.

CYBER Fixed Module Drive
Learning Activity 3-B

Directions: Each of the following statements describes one of the fields listed below. After reading each statement, write the letter of the function it describes in the blank preceding it.

	<u>Statement</u>	<u>Field</u>
<u>C</u>	21. Contains cylinder, head, and sector numbers.	a. Sync pattern
<u>d</u>	22. Provides error detection when reading.	b. Sync byte
<u>a</u>	23. Synchronizes the read logic to the speed of the disk pack.	c. Address
<u>2</u>	24. Provides storage of data.	d. Checkword
<u>G</u>	25. Compensates for speed variation.	e. Data
<u>B</u>	26. Alerts the logic that a data or an address field is approaching.	f. End of record
<u>F</u>	27. Provides checkword protection.	g. Tolerance gap

Directions: Read each of the following statements. Place a T in the appropriate blank if the statement is true and an F if the statement is false.

<u>T</u>	28. The pack serial number is recorded in the data field of sector zero, head zero, cylinder 841.
<u>F</u>	29. The utility flaw map is located at cylinder zero, head zero, sector zero.
<u>T</u>	30. Cylinder 841, head 0, the data field of sector 1 contains a list of factory defective tracks.

CYBER Fixed Module Drive
Learning Activity 3-B

ANSWERS TO LEARNING ACTIVITY 3-B.

Now correct your answers. If you make any errors, you may wish to review before going on to learning activity 3-C.

- | | |
|---|-------------------------------|
| 1. write, read or read, write | 15. 25 |
| 2. MFM or modified frequency modulation | 16. two |
| 3. head disk assembly | 17. 32 and 33 |
| 4. cylinder | 18. head or track, and sector |
| 5. track | 19. 31 |
| 6. four | 20. cylinder |
| 7. two | 21. c |
| 8. 1688, 844 for each head | 22. d |
| 9. 843 (844 cylinders, numbered 0 outermost to 843 innermost) | 23. a |
| 10. 96, bottom | 24. e |
| 11. do not | 25. g |
| 12. is not | 26. b |
| 13. 34 | 27. f |
| 14. logical | 28. T |
| | 29. F |
| | 30. T |

LEARNING ACTIVITY 3-C. TEXT READING: SERVO DISK ELEMENTS

This activity describes the elements of the servo disk, servo pulses, servo bytes, index, servo zones, and servo-to-data surface correlation.

OBJECTIVE

- You will be able to list the major elements of the 885 Fixed Module Drive servo disk and describe the function of each.

The servo disk surface is a special disk surface that is recorded when the pack is manufactured. There is only one head on the servo head arm assembly, and it is a read-only head.

The information read from the servo surface provides both the timing signals and positioning information. Sector marks are generated to divide the data tracks into 34 physical sectors. Index marks are generated once per revolution to provide a reference timing mark. Motor-at-speed is generated when the pack is rotating at 3600 rpm. Clock signals are generated for use during the data transfer operations. Track crossing signals and analog feedback voltages are generated to control the closed loop servo positioning logic.

The servo disk surface is recorded with 932 bands or tracks. The band is recorded with pulses arranged in units called servo bytes. There is space for six pulses in a servo byte (see figures 3-18 and 3-19).

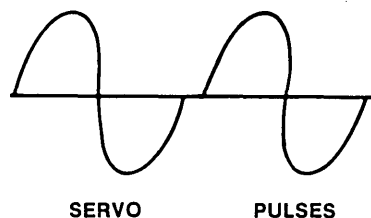


Figure 3-18. Servo Pulses

CYBER Fixed Module Drive
Learning Activity 3-C

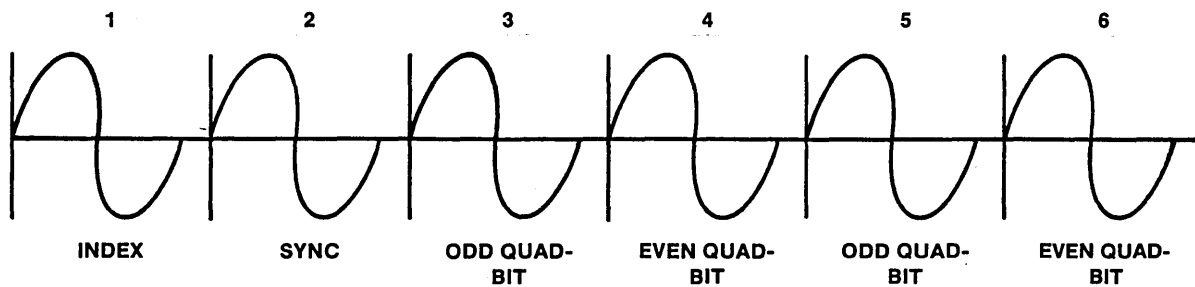


Figure 3-19. Servo Byte

The first pulse is called the index pulse (not the index mark that occurs once per revolution). The second pulse is called a sync pulse; the third and fifth pulses (odd numbers) are called odd quad bits; the fourth and sixth pulses (even numbers) are called even quad bits. There are four pulses after the sync pulse, hence the name quad, meaning four. Any one servo byte will have either the odd or even quad bits present.

A servo byte has space for six pulses but never has more than four pulses.

A servo byte with only odd quad bit pulses present is called an odd servo byte (see figure 3-20).

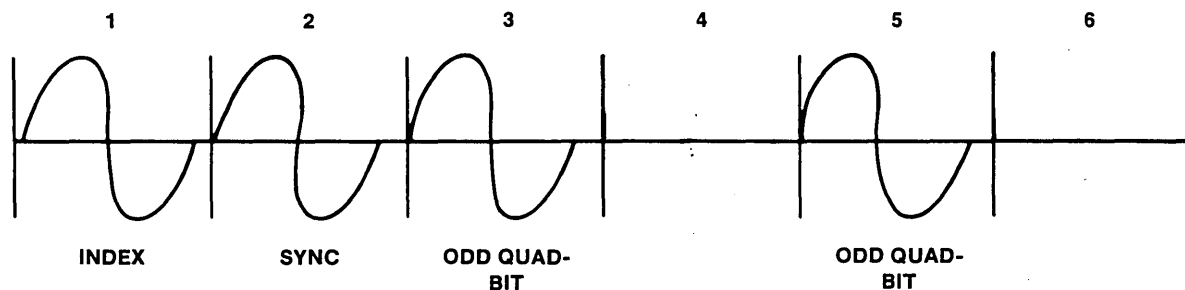


Figure 3-20. Odd Servo Byte

A servo byte with only even quad bit pulses present bit is called an even servo byte (see figure 3-21).

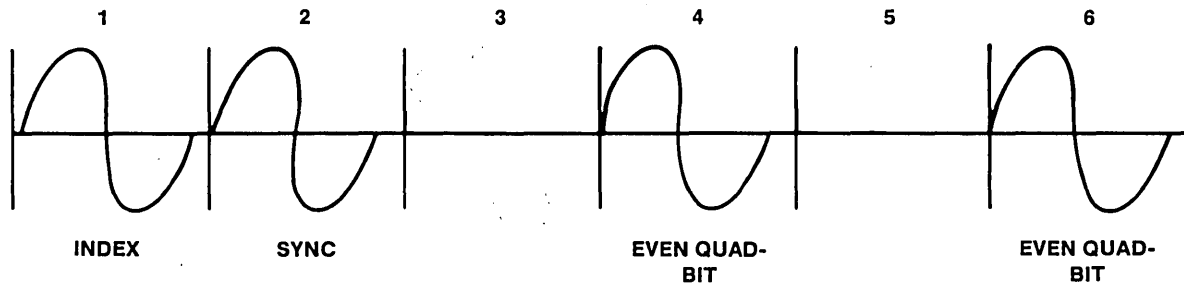


Figure 3-21. Even Servo Byte

The servo surface is recorded with a band of all even servo bytes and then a band of all odd servo bytes for a total of 932 bands (see figure 3-22).

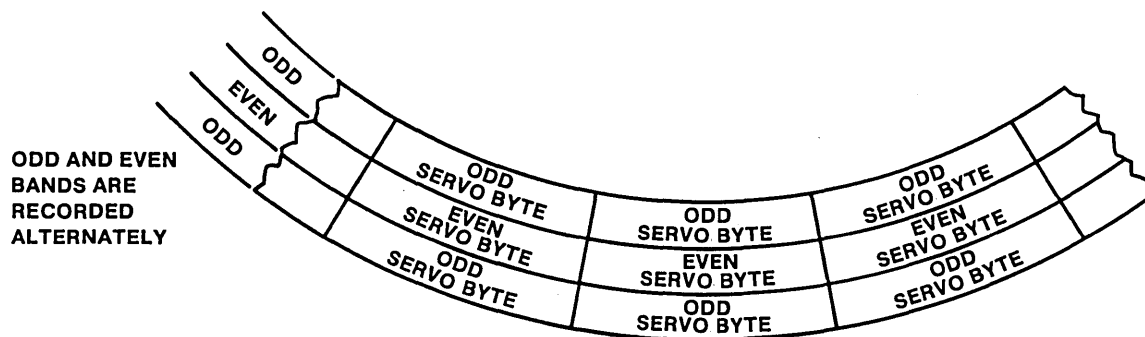


Figure 3-22. Servo Bands

Each band recorded on the servo disk surface has a series of five special servo bytes. The index pulse is missing on the second, fourth, and fifth servo byte. This index pattern is located at the same place on each band. It effectively produces a line that

CYBER Fixed Module Drive
Learning Activity 3-C

extends from the inner to the outer edge of the servo surface. The read-only servo head reads the index pattern once per revolution when at any position on the servo surface. The FMD logic monitors the information from the servo head and generates a signal called index or index mark when the index pattern is detected. The index mark is the reference timing pulse for the clock circuits in the FMD device and controller (see figure 3-23).

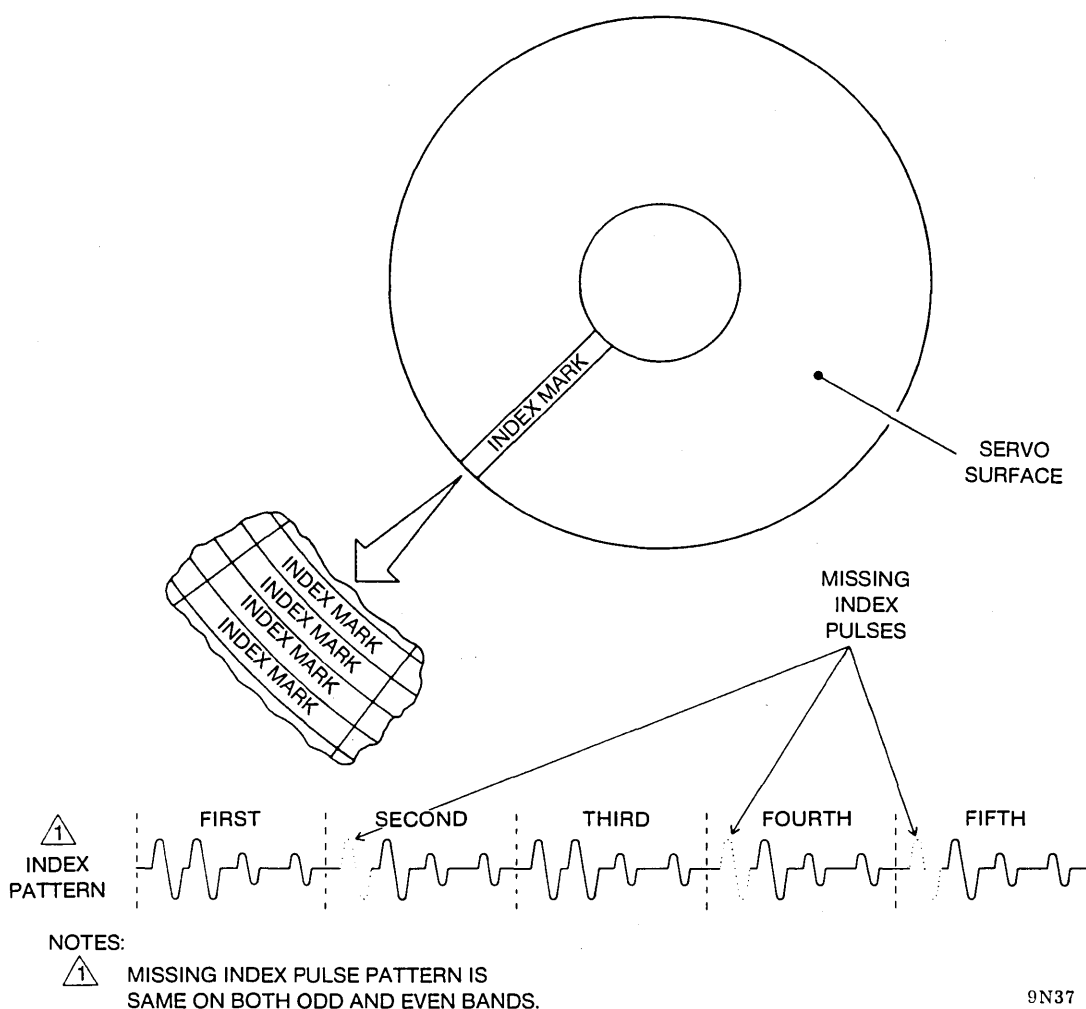


Figure 3-23. Index Mark Pattern

The servo disk surface is divided into zones or bands. The servo bytes are encoded differently in each zone. The term band is used to describe one track of servo bytes. The term guard band is used to describe a zone on the servo surface with more than one band encoded with specific patterns.

There is a blank area between outer guard band 2 and the edge of the disk. Before the disk pack rotation is stopped, the servo head is moved to the outer edge of outer guard band 2. It is called the home position (see figure 3-24).

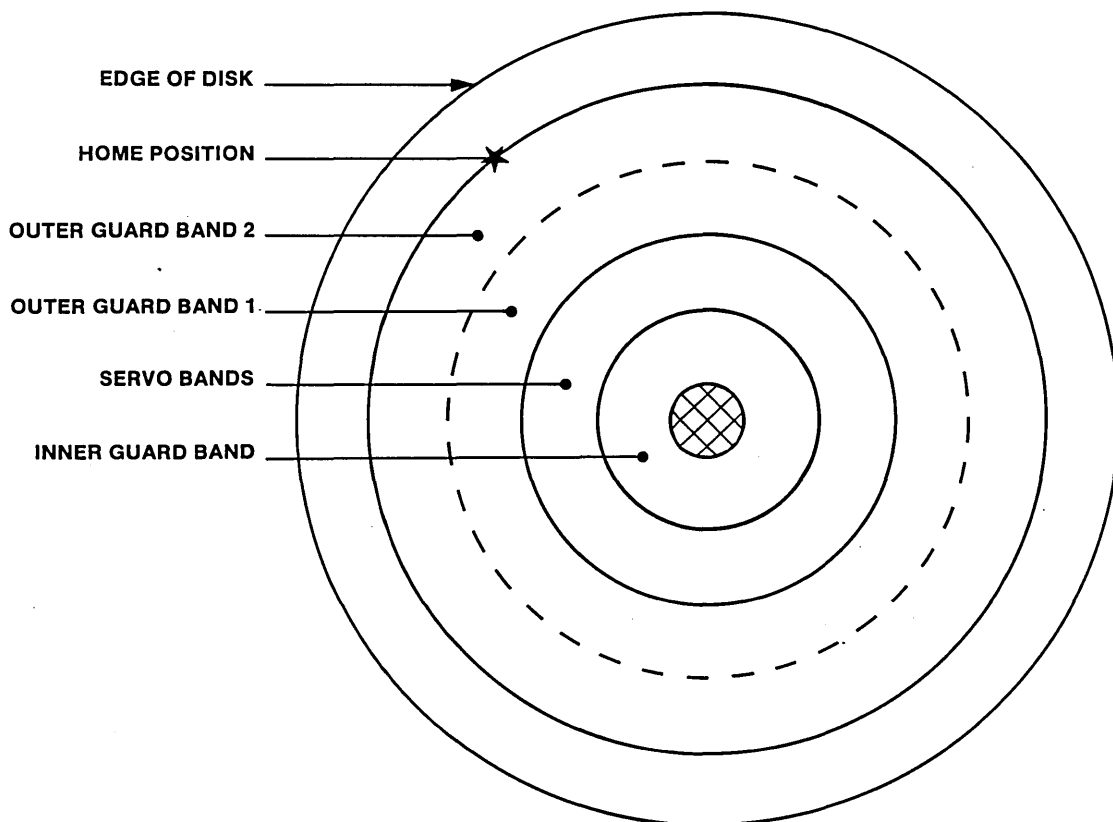


Figure 3-24. Servo Zones

CYBER Fixed Module Drive
Learning Activity 3-C

The zone closest to the outer edge of the disk is outer guard band 2. The zone goes from track number -56, the outermost track, to track number -13, the innermost track in the band (see figure 3-25).

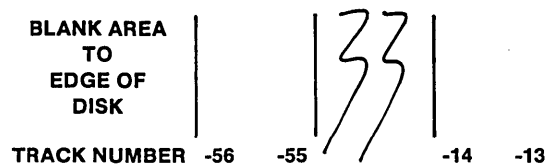


Figure 3-25. Outer Guard Band 2

Each band, in outer guard band 2, is divided into 78 equally spaced segments (also called sectors but not the same as a data sector). Each segment contains 64 servo bytes. The first five bytes of each segment are servo bytes. The index pulse is missing on the second, third, and fourth servo byte (see figure 3-26).

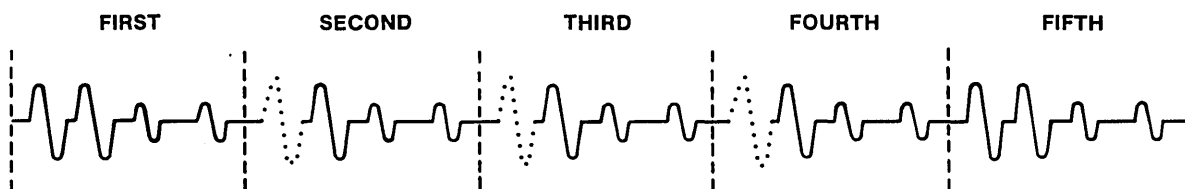


Figure 3-26. Guard Band 2 Byte

Going toward the center of the disk from track -13 to track number -3 is outer guard band 1 (see figure 3-27).

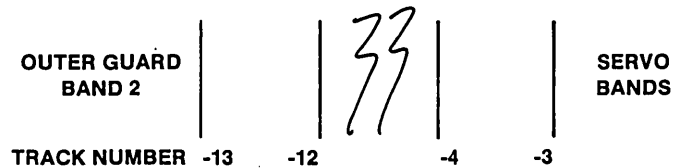


Figure 3-27. Outer Guard Band 1

Each band is divided into 78 equally spaced segments that contain 64 servo bytes. The first five bytes of each segment are servo bytes. The index pulse is missing on the second and fourth servo byte (see figure 3-28).

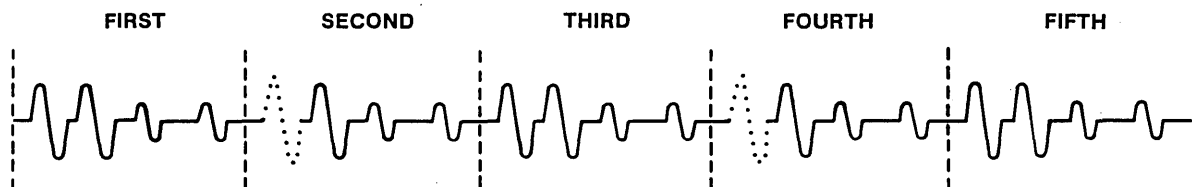


Figure 3-28. Guard Band 1 Byte

CYBER Fixed Module Drive
Learning Activity 3-C

Moving toward the center of the disk from track number -3 to track number 0 are three bands of even servo bytes. The three bands are not divided into segments but consist of 4992 even servo bytes from index mark to index mark (see figure 3-29).

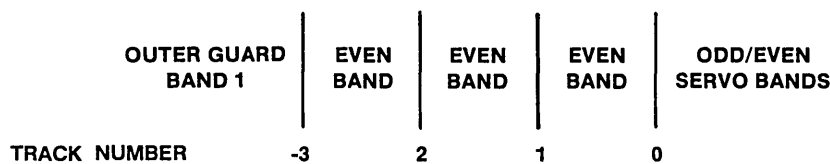


Figure 3-29. Servo Bands - Even Bytes

Moving toward the center of the disk from track number 0 to track number 843 are alternate bands of odd and even servo bytes. The bands are not divided into segments but consist of 4992 servo bytes from index mark to index mark. This is the zone of the servo surface where the servo head can stop for a total of 844 stopping positions (see figure 3-30). When the servo head is at a stopping position, it is centered between an odd and even servo band. For example, when the carriage is at cylinder or track zero, the servo head is actually centered between the innermost of the three even bands and the outermost odd band of the odd/even servo band.

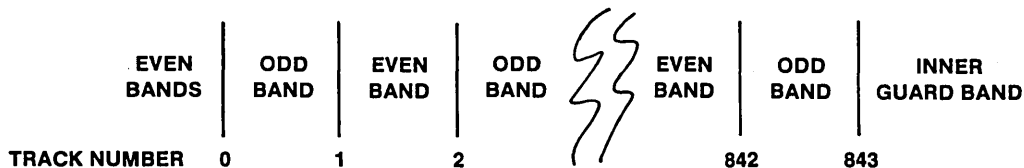


Figure 3-30. Servo Bands - Odd/Even Bands

Because there are two data heads on each data surface, the servo head and data heads are not physically aligned directly over each other when the servo head is positioned at a cylinder address. When the servo head is stopped in the odd/even servo band, the two data heads define two tracks on each data disk surface. The 844 data tracks for one head do not overlap the 844 data tracks of the other head on the same data disk surface. Only when the servo head is in the odd/even servo band are the data heads over the data recording area of the disk surface (see figure 3-31).

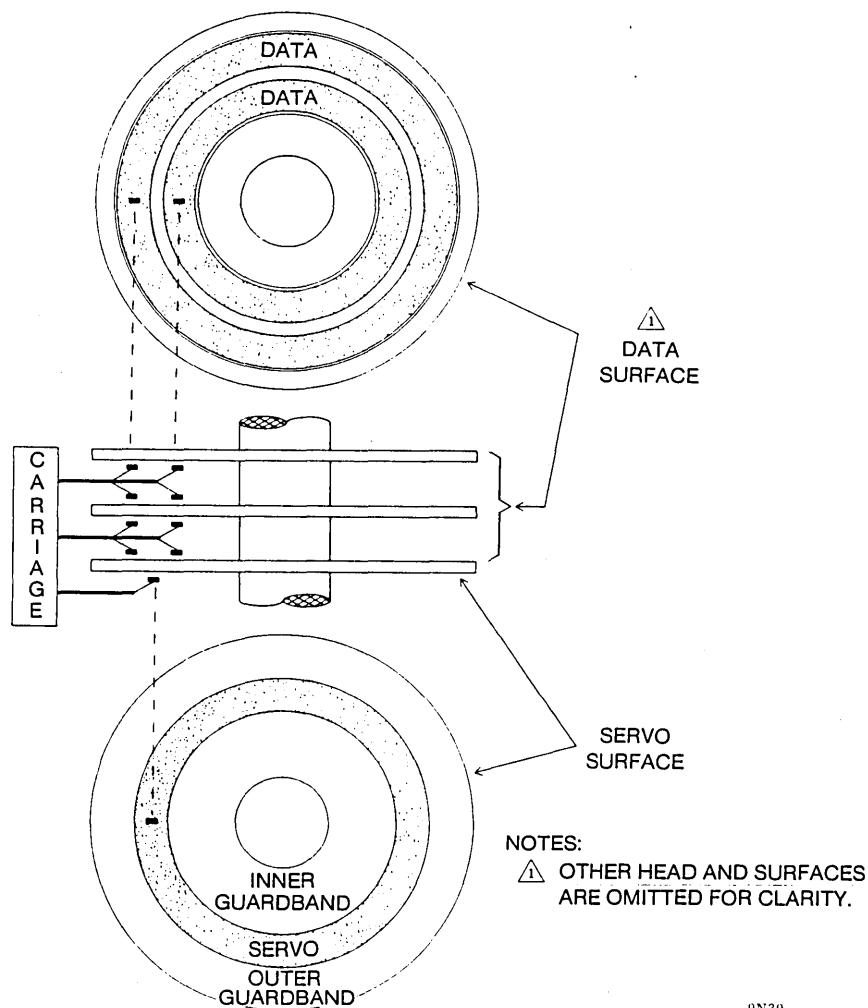


Figure 3-31. Servo-to-Data Surface Correlation

CYBER Fixed Module Drive
Learning Activity 3-C

Moving toward the center of the disk from track number 843 to track number 875 is the inner guard band (see figure 3-32).

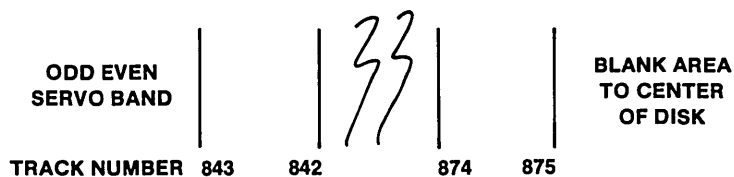


Figure 3-32. Inner Guard Band

Each track is divided into 78 equally spaced segments that contain 64 servo bytes. The first five bytes of each segment are servo bytes. The index pulse is missing on the first, fourth, and fifth servo byte (see figure 3-33).

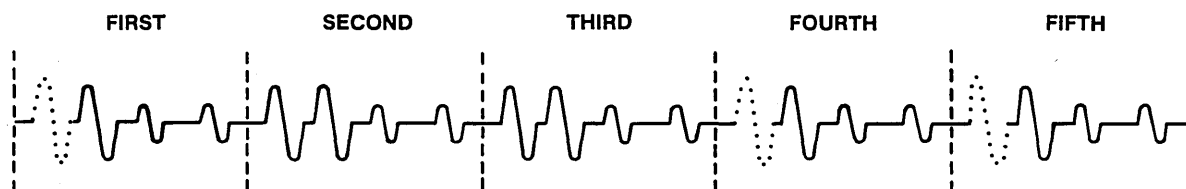


Figure 3-33. Inner Guard Band Byte

CYBER Fixed Module Drive
Learning Activity 3-C

The logic of the FMD monitors the information read from the prerecorded servo disk surface. The logic determines that the carriage is outside of the data fields when the inner or outer guard band patterns are detected.

In a later learning activity, you will see how the information from the servo disk surface is used in the logic operations of the FMD unit.

This concludes learning activity 3-C. You may review this activity if you have questions.

LEARNING ACTIVITY 3-D. REFERENCE READING: SERVO DISK

This activity describes the elements of the servo disk, servo bands and bytes, servo zones, and servo-to-data surface correlation.

OBJECTIVE

- You will be able to list major elements of the 885 Fixed Module Drive servo disk and describe the function of each.

Read in section 3 of the CYBER Disk Storage BZ703 Theory of Operation Manual, publication number 83322880, the paragraphs under Servo Disk entitled General, Servo Bands and Bytes, Servo Zones, and Servo-to-Data Surface Correlation. Study figures 3-15 through 3-20. (Figures 3-17 through 3-22 if Manual is Rev. C or later.)

LEARNING ACTIVITY 3-E. EXERCISE: SERVO DISK ELEMENTS REVIEW

This activity reviews the fixed module drive servo disk elements. After completing the exercise, check your answers with those given at the end of this learning activity.

OBJECTIVE

- You will be able to list the major elements of the 885 Fixed Module Drive servo disk and describe the function of each.

Directions: After reading each of the following statements, fill in the blank(s) with a word or words to complete the statement and make it true.

1. The servo disk surface is (is/is not) recorded when the pack is manufactured.
2. A servo band is recorded with pulses arranged in units called servo bytes.
3. The first pulse in the servo byte is called a index pulse.
4. An odd servo byte has one index pulse, one sync pulse, and 2 odd quad bit pulses.
5. The second pulse in the servo byte is called a sync pulse.
6. An even servo byte has even quad bit pulses.
7. The index mark pattern occurs once per revolution of the disk pack.
8. The index pattern consists of 5 servo bytes.
9. The index pulse is missing in the second, fourth, and fifth servo bytes of the index pattern.
10. The FMD logic generates a signal called index from the index pattern.
11. The outermost zone on the servo disk is called outer guard band 2.

CYBER Fixed Module Drive
Learning Activity 3-E

12. When the servo head is in outer guard band 1, the data heads are not (are/are not) over their data tracks.
13. The index pulse is missing in the second, third, and fourth servo bytes of the outer guard band 2 pattern.
14. The three bands from track-3 to 0 are all even (odd/even) bands.
15. The servo head is between an odd servo band and an even servo band when stopped at a cylinder address.
16. The outer and inner guard bands are divided into 28 equally spaced sectors or segments.
17. The odd/even servo bands have 4992 servo bytes.
18. Track number -56 is the outermost (innermost/outermost) track on the servo disk surface.
19. The inner guard band track closest to the center of the disk is track number 875.
20. When the servo head is positioned from track 0 through 843 the data heads are (are/are not) over their data tracks.
21. When disk pack rotation is stopped, the servo head is positioned to the outer edge of outer guard band -56. The servo head is at the home position.

CYBER Fixed Module Drive
Learning Activity 3-E

The answers to this learning activity are on the following page.

CYBER Fixed Module Drive
Learning Activity 3-E

ANSWERS TO LEARNING ACTIVITY 3-E

Now correct your answers.

1. is
2. bytes
3. index
4. two
5. sync
6. even
7. once
8. five
9. fourth and fifth
10. index or index mark
11. guard band 2
12. are not
13. third and fourth
14. even
15. centered between
16. 78
17. 4992
18. outermost
19. 875
20. are
21. two, home

LEARNING ACTIVITY 3-F. TEXT READING: FUNCTIONAL DIAGRAMS

This activity describes the functional areas of the FMD basic and unit functional block diagrams.

OBJECTIVE

- You will be able to list the major functional areas of the 885 Fixed Module Drive block diagrams and describe the function of each.

Figure 3-34 is a basic functional diagram of the device. Functions shown above the dashed line in the figure are duplicated in each device; the hardware components corresponding to these duplicated functions are referred to as device A and device B. Functions below the dashed line are used in common by both devices. Thus, the CDC CYBER disk storage unit can function as two separate devices, while using some components in common.

CYBER Fixed Module Drive Learning Activity 3-F

The AC power consists of 50 or 60 Hz and 400 Hz. The blower and drive motors use the 50/60 Hz. The DC logic voltages are generated from 400 Hz. The power sequence circuits of all devices function in a specific order to enable power to all of the drive motors to prevent overload of the site power source. The controller selects one of the A or B functional segments (devices) for storing or retrieving data in the HDA mounted on the respective deck assembly. The controller places control commands and signals on the lines to the device to move the read/write heads in the HDA to a specified position. The commands are decoded and used by the servo circuit to position the heads to the desired location. The device notifies the controller via the status lines when the positioning is complete. The controller commands data to be stored at or retrieved from a particular address in the HDA. When the read or write operation is complete, the controller may command the device to move the heads to a new location. Upon request, the device sends status information to the controller.

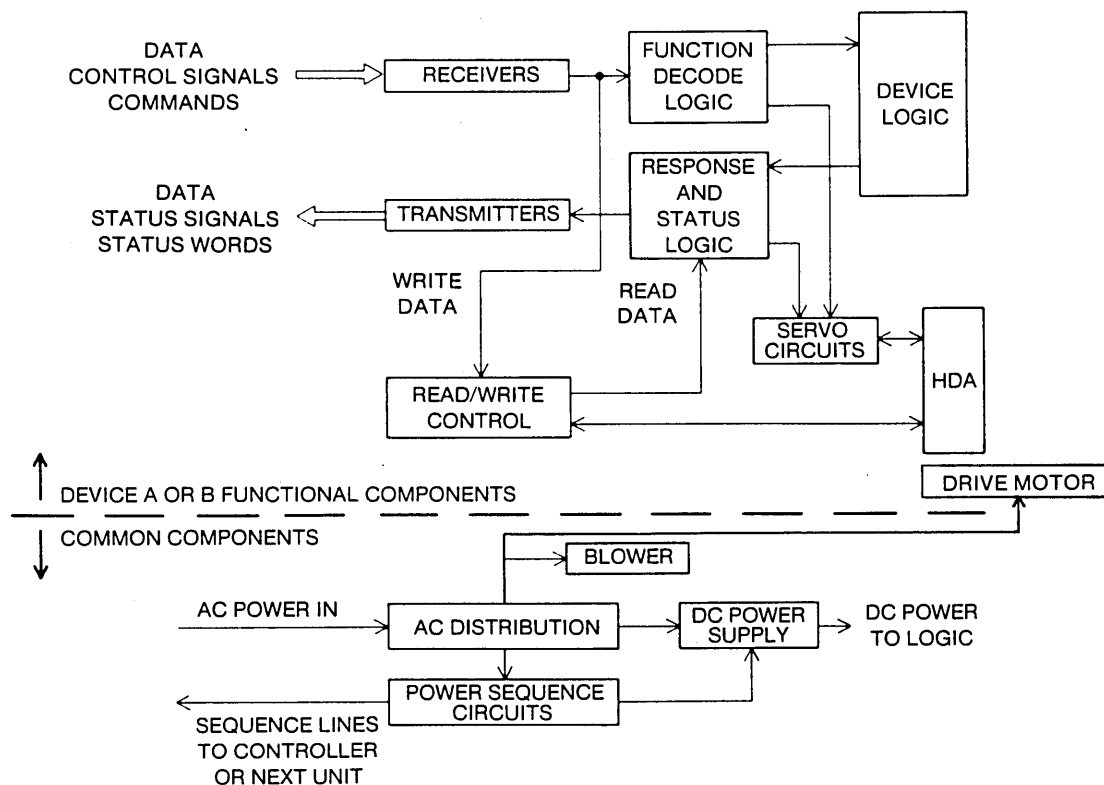


Figure 3-34. Basic Functional Diagram

Figure 3-35 is another simplified block diagram that further illustrates the basic functions of the unit.

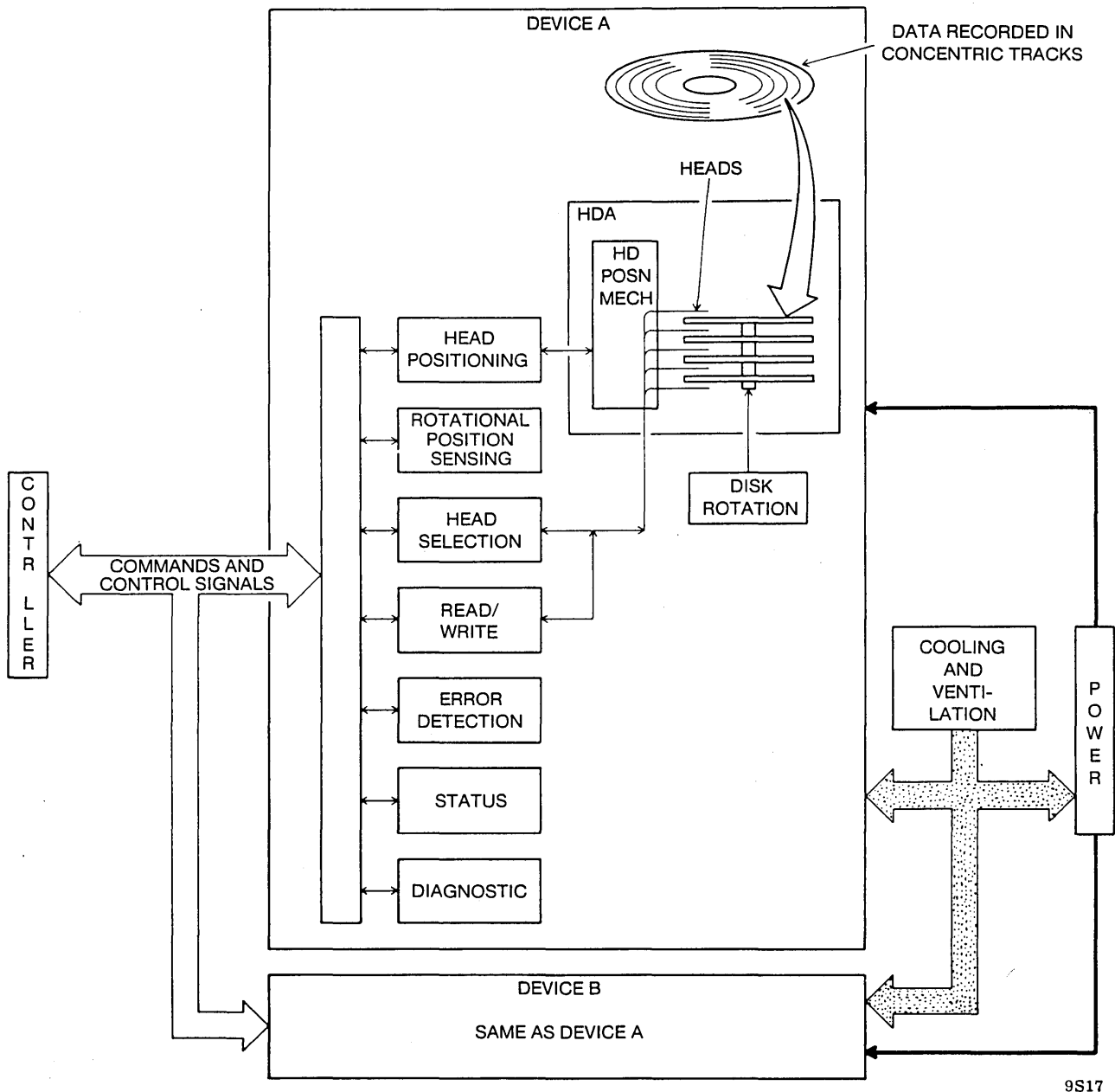
The power system provides all the power required by the unit.

Sequencing signals from the controller along with switches within the unit control operation of the power system.

The unit must be ventilated and cooled to operate properly. This ventilation and cooling is provided by air from the air flow system.

Device A and device B are the unit elements that actually perform the writing and reading of data. These devices are independent of each other, but they contain identical hardware and perform identical operations.

CYBER Fixed Module Drive
Learning Activity 3-F



9S17

Figure 3-35. Unit Functional Block Diagram

A device stores data on disks located within the HDA. Reading and writing is performed by electromagnetic devices called heads (also located within the HDA) positioned over the disk surfaces. There are two separate heads for each disk surface in the HDA. The device positions the heads in such a way that data is written in concentric tracks.

During operation, the heads do not actually touch the disk surfaces. Instead, they fly over them on a cushion of air created by the rotation of the disks at a speed of 3600 rpms. The disk rotation system provides the energy to rotate the disks.

A device operates under direction of the controller; communication for those instructions is completed via the interface. The interface consists of a number of signal lines that carry commands to the device and those that return status back to the controller.

Some interface lines, including those that carry commands, are not enabled unless the controller first selects the device. Selection allows the controller (which connects to more than one device) to initiate and direct the operation of a specific device.

Before a read or write operation can be performed, the controller must prepare the device for the operation. This involves enabling the head located over the proper disk surface (head selection), moving the heads to the proper track (head positioning), and locating the segment of the track (sector) where the data is to be read or written (rotational position sensing).

When the head selection, positioning, and sector selection functions are complete, the controller commands the device to actually write or read the data. During a write operation, the device receives data from the controller, processes it, and finally, writes it on the disk. The device recovers data from the pack and transmits it to the controller in a subsequent read operation.

The device checks for error conditions during all operations. If it detects an error, the device signals the controller and/or lights a fault indicator on the maintenance panel. In addition to error checking, the device monitors the status of operations as they progress. By requesting this status before or after an operation, the controller determines the state of the device.

The device also has a diagnostic function that allows the controller to cause certain intentional error conditions within the device. The results of these errors are useful in troubleshooting.

CYBER Fixed Module Drive
Learning Activity 3-G

LEARNING ACTIVITY 3-G. EXERCISE: FUNCTIONAL DIAGRAM REVIEW

This activity reviews the fixed module drive functional block diagrams.

OBJECTIVE

- You will be able to list the major functional areas of the 885 Fixed Module Drive block diagrams and describe the function of each.

After completing the exercise, check your answers with those given at the end of this learning activity.

Directions: After reading each of the following statements on the basic functional block diagram, fill in the blank to indicate whether the component is a common or a device component.

1. HDA Device.
2. Blower Common.
3. AC distribution Common.
4. Read/write control Device.
5. Servo circuits Device.
6. Device logic Device.
7. DC power supply Common.
8. Power sequence circuits Common.

Directions: After reading each of the following statements on the basic functional block diagram, fill in the blank(s) with a word or words to complete the statement and make it true.

9. Data from the controller passes through the receivers, then the Read write control to the HDA.

CYBER Fixed Module Drive
Learning Activity 3-G

10. The path of data to the controller is from the HDA to the read/write control, response and status logic, then to the transmitters to the data lines to the controller.
11. The servo circuits control positioning the heads to the desired location on the disk surface.
12. The AC distribution supplies power to the blower drive motor, DC power supplies, and power sequence circuits.

Directions: Read each of the following statements on the unit functional block diagram. Place a T in the appropriate blank if the statement is true and an F if the statement is false.

- True 13. Device A and device B are independent of each other, but they contain identical hardware and perform identical operations.
- False 14. The device recovers data from the pack and transmits it to the controller on a write operation.
- False 15. The disk rotation element is shared by device A and device B.

Directions: Each of the following statements describes one of the unit functional block diagram functional areas listed below. After reading each statement, write the letter of the functional area it describes in the blank preceding it.

- | <u>Statement</u> | <u>Functional Areas</u> |
|--|--------------------------------|
| <u>b</u> 16. Locates the segment of the track where the data is to be read or written. | a. Head selection |
| <u>e</u> 17. Initiates and directs the operation of a specific device. | b. Rotational position sensing |
| <u>a</u> 18. Enables the head for reading or writing. | c. Head positioning |
| <u>C</u> 19. Controls moving the heads to the proper cylinder. | d. HDA |
| <u>d</u> 20. Contains disks for storing data. | e. Controller |

CYBER Fixed Module Drive
Learning Activity 3-G

ANSWERS TO LEARNING ACTIVITY 3-G

1. device
2. common
3. common
4. device
5. device
6. device
7. common
8. common
9. read/write control
10. read/write control, status
11. servo circuits
12. blower, DC power supply, drive motor, etc.
13. true
14. false
15. false
16. b.
17. e
18. a
19. c
20. d

LEARNING ACTIVITY 3-H. TEXT READING: I/O COMMANDS

This activity describes the control and status commands and the purpose of each interface signal.

OBJECTIVE

- You will be able to name the controller to the 885 Fixed Module Drive commands and interface signals and describe their purpose.

Each FMD device is connected to the controller by one I/O cable. If the FMD device has the dual channel option, there will be two identical I/O cables, one for each channel.

Commands, data, and control signals are sent to the device from the controller. Status information and data are sent to the controller from the device. Four lines are used only for control signals to the device from the controller (see figure 3-36).

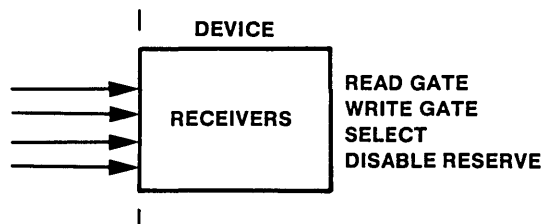


Figure 3-36. Device Receivers

The Select signal is sent by the controller to the device it wants to reserve for any operation.

The Disable Reserve is used by the controller on a dual channel device to deselect the opposite channels reserved condition.

CYBER Fixed Module Drive
Learning Activity 3-H

The Read and Write gates in conjunction with control select are used to enable read or write operations to occur. Six lines are used only for status signals to the controller from the device (see figure 3-37).

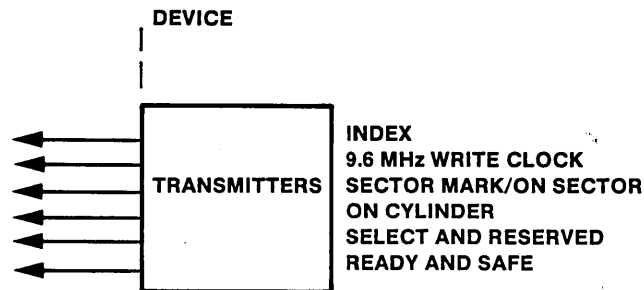


Figure 3-37. Device Transmitters

The Index signal is generated once per revolution from the index mark pattern on the servo disk surface.

The 9.6 MHz Write Clock is part of the servo clocks generated from the servo disk surface. It is used by the controller during write operations to synchronize the write data transfer to the rotational speed of the disk.

The Sector Mark is generated by the logic counting servo clocks. So many counts equal a sector mark. There are 34 physical sectors per revolution. The On Sector signal is generated when the count in the sector mark counter compares with the sector requested by the controller. There is only one on sector condition per revolution.

The On Cylinder signal is generated when the carriage is stopped at any of the 844 stopping positions or cylinders.

The Select and Reserved signal is sent to the controller as the device's response to a successful controller to device select operation.

The Ready and Safe signal is present when the device is on cylinder and there are no disabling error conditions present.

Ten bidirectional lines are used for transferring information both to and from the device (see figure 3-38).

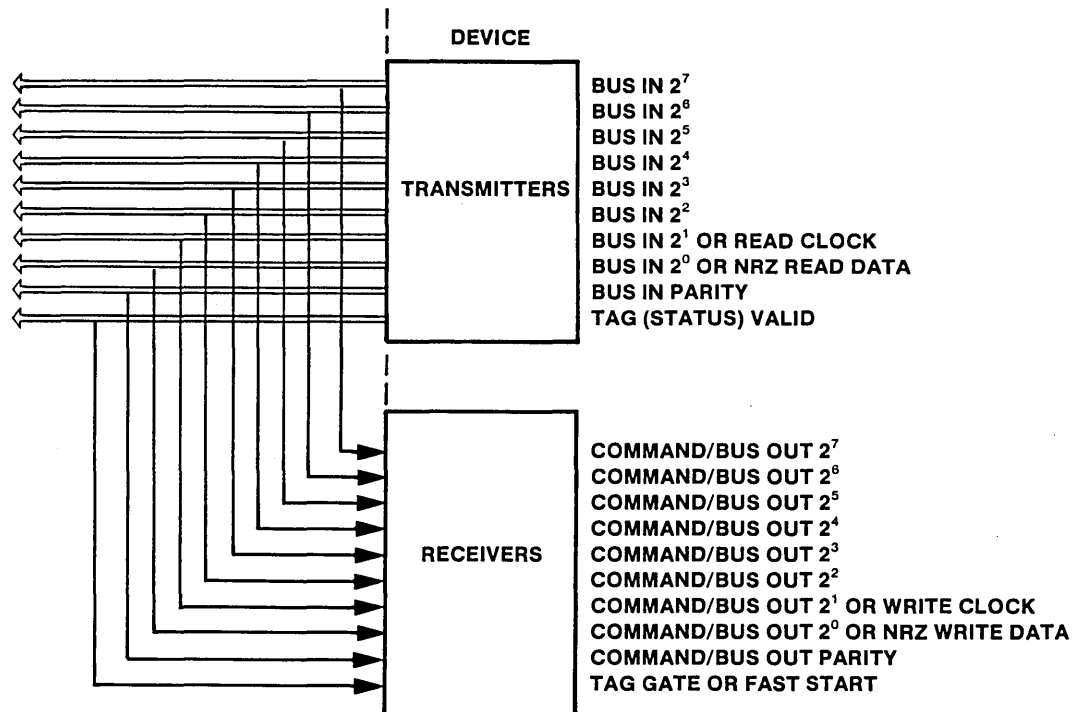


Figure 3-38. Bidirectional Lines

The basic unit of information is the byte. A byte consists of eight information bits (logical 1 or 0) plus a parity bit. Bit position 0 in the byte is always the least significant bit. The parity bit will be a logical one if the number of one bits is even. Data is transferred between a device and the controller one byte at a time in a parallel format. Eight data lines plus one parity line to check for odd parity are used to transmit commands to the device.

CYBER Fixed Module Drive
Learning Activity 3-H

The Tag Gate signal is used to gate the command code into the device logic where it's decoded. For example, a code of (0100 0100) 44 hex decodes as Load Head Register. Now the device needs to know which head to select. Immediately following the command, the controller places the head address on the same nine lines now called the bus-out information. The bus-out information is gated into device logic by a second tag gate signal. The logic uses the command and bus-out information to perform the operation.

The device logic also takes the command and bus-out information and sets up a status word, eight bits plus parity, on the bus-in transmitters for the same nine lines to the controller. A Tag (status) Valid signal is used to gate the bus-in status word into the controller.

Five of the bidirectional lines have additional functions during data transfer operations. During write operations, bus-out lines 2⁰ and 2¹ carry the non-return to zero (NRZ) Write Data and Write Clock signals. The write clock is used to gate the NRZ data into the device logic. The logic converts the NRZ write data to MFM format for writing in the selected sector. During read operations, a signal called Fast Start is issued on the tag gate line. The fast start signal is generated by the controller during the sync pattern 2 before reading the data field. The device logic takes the MFM read data, converts it into NRZ data, and generates a clock signal. The Read Clock is used to clock the NRZ Read Data into the controller logic. The NRZ read data and read clock are sent to the controller on bus in lines 2⁰ and 2¹.

This completes learning activity 3-H. You may review any portion of the learning activity if you have questions.

LEARNING ACTIVITY 3-I. REFERENCE READING: COMMANDS AND SIGNALS

This activity lists and describes all 4X and 8X commands and all controller/device signal lines.

OBJECTIVE

- You will be able to name the controller to the 885 Fixed Module Drive commands and interface signals and describe their purpose.

In the CYBER Disk Storage BZ703 Theory of Operation Manual, publication number 83322880, see figures 3-12 and 3-13 for a list of all commands. The 4X commands are called control commands. Figure 3-12 lists all control commands and the purpose of each bit of the bus-out and bus-in lines. The 8X commands are called status commands. Figure 3-13 lists all status commands and bus bits. See table 3-3 and 3-4 for a description of all control and status commands. See tables 3-1 and 3-2 for a description of all I/O signal lines. Table 3-1 describes the controller to device signal lines. Table 3-2 describes the device to controller signal lines. All of the above tables and figures are in the CYBER Disk Storage BZ703 Theory of Operation Manual, publication number 83322880.

NOTE: If Manual is Rev. C or later, use Figure 3-14 and 3-15 in place of figure 3-12 and 3-13.

LEARNING ACTIVITY 3-J. EXERCISE: I/O COMMANDS REVIEW

This activity reviews the fixed module drive I/O commands and Interface signals. After completing the exercise, check your answers with those given at the end of this learning activity.

OBJECTIVE

- You will be able to name the controller to the 885 Fixed Module Drive commands and interface signals and describe their purpose.

Directions: Each of the following statements describes one of the I/O signals listed below. After reading each statement, write the letter of the I/O signal it describes in the blank preceding it.

	<u>Statement</u>	<u>I/O Signals</u>
<u>2</u>	1. Sent by the controller to the device it wants to reserve.	a. Write gate b. Index
<u>a</u>	2. With control select enables a write operation.	c. Bus-in lines d. Select
<u>2</u>	3. Signal that occurs once per revolution.	e. On cylinder
<u>C</u>	4. Carries status and read information to controller.	
<u>2</u>	5. Signal that indicates the carriage is not positioning.	

Directions: After reading each of the following statements, fill in the blank(s) with a word or words to complete the statement and make it true.

6. A control command of 46 hex decodes as set control select.
7. To load cylinder register lower, the controller issues a hex code of 41.

CYBER Fixed Module Drive
Learning Activity 3-J

8. The lower cylinder address is sent to the device on the bus out lines.
9. The nine bus-in lines are bits 2^0 through 2^7 and parity.
10. The control command is a binary code of 01001010, this decodes as a 4A - Clear Fault command.
11. For the controller to receive status word 1, it must issue a status command of 88 hex.
12. Bit one of status word one is set, this indicates that the device start switch is on.
13. Bit 6 of status word 3 is set to indicate that an outer guard pattern has been detected.
14. Bit one of status word five is set to indicate failure to decode index mark.
15. The Tag Gate signal is issued twice for each control command or status command sequence.

CYBER Fixed Module Drive
Learning Activity 3-J

ANSWERS TO LEARNING ACTIVITY 3-J

1. d
2. a
3. b
4. c
5. e
6. set control
7. 41
8. bus-out or command/bus-out lines
9. parity
10. clear fault
11. 88
12. start switch
13. guard band
14. index mark
15. twice

LEARNING ACTIVITY 3-K. AUDIOTAPE: DETAILED BLOCK DIAGRAM

This activity describes the detailed block diagram of the FMD logic.

OBJECTIVE

- You will be able to list the major functional areas of the 885 Fixed Module Drive detailed block diagram and describe the purpose of each area.

The detailed block diagram is shown in figures 3-39 through 3-45. Notice that different areas on each page are highlighted. As you listen, the tape will describe the highlighted areas in each figure. You may stop the tape at any time to take notes or go over some topics.

Load the audiotape Detailed Block Diagram (75445258) into your cassette player and turn to the block diagram in figure 3-39.

NOTE

Appendix D contains the script of this audiotape.

STUDENT NOTES

Figure 3-39. Detailed Block Diagram - Reserved

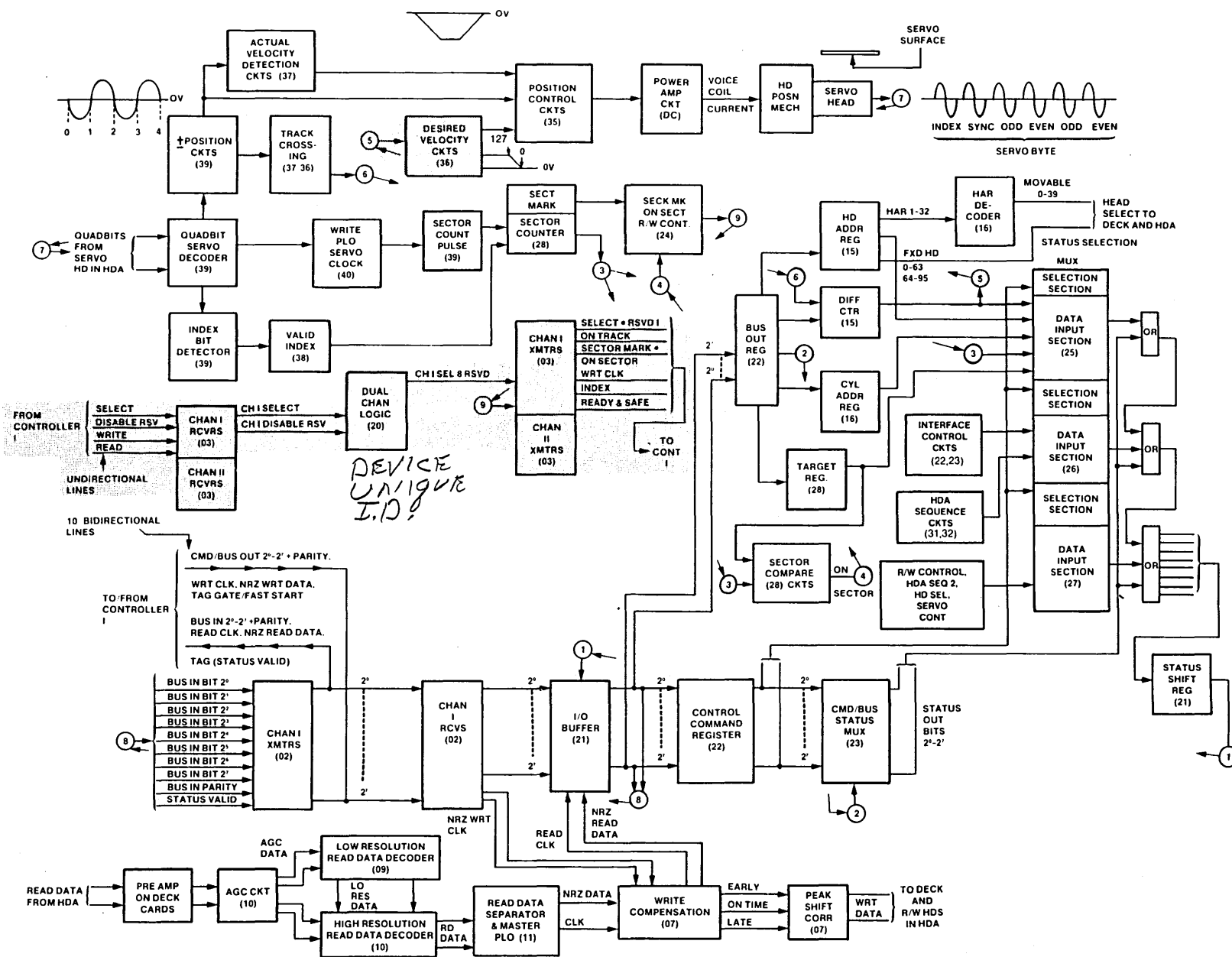


Figure 3-40. Detailed Block Diagram - Commands

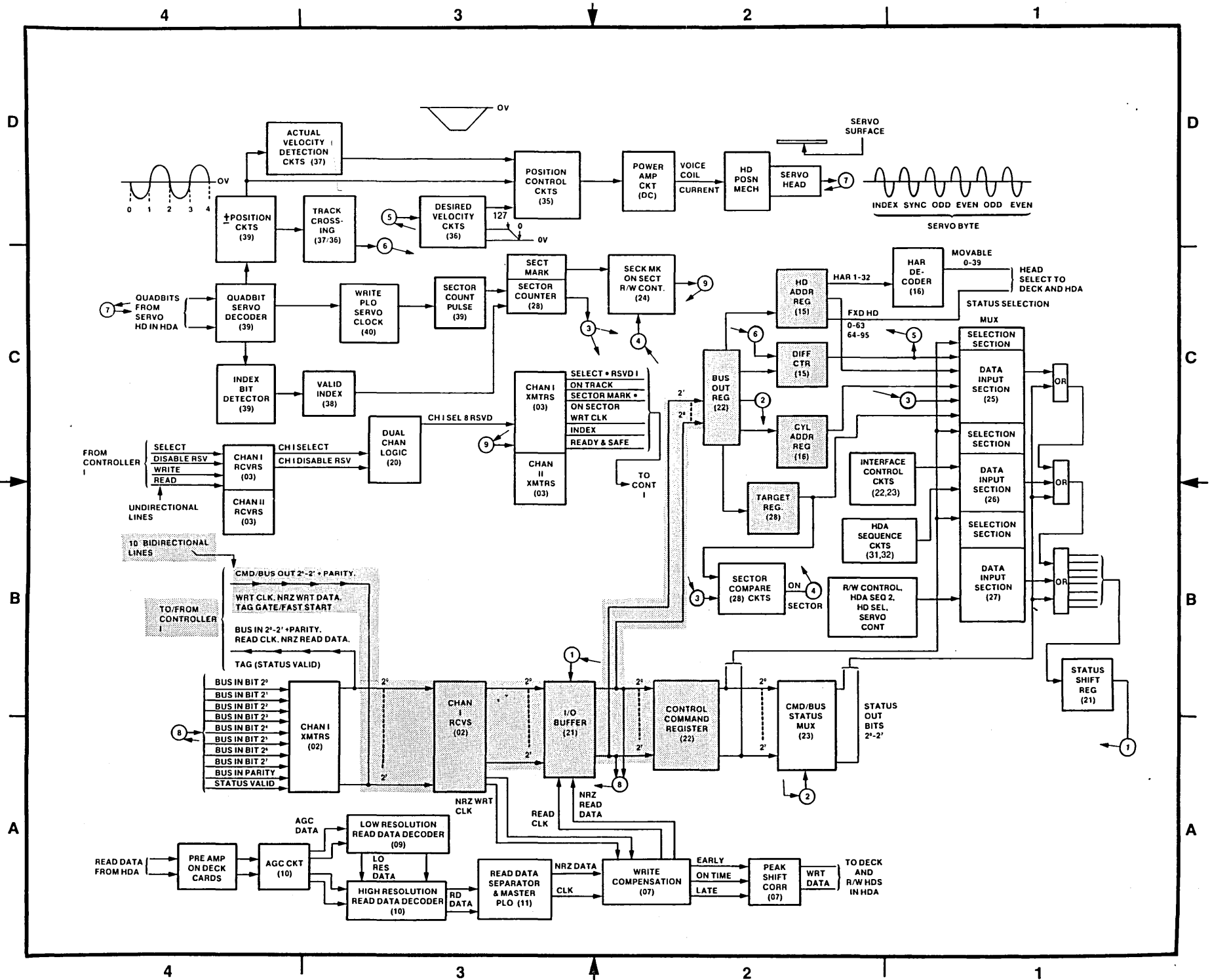


Figure 3-41. Detailed Block Diagram - Status

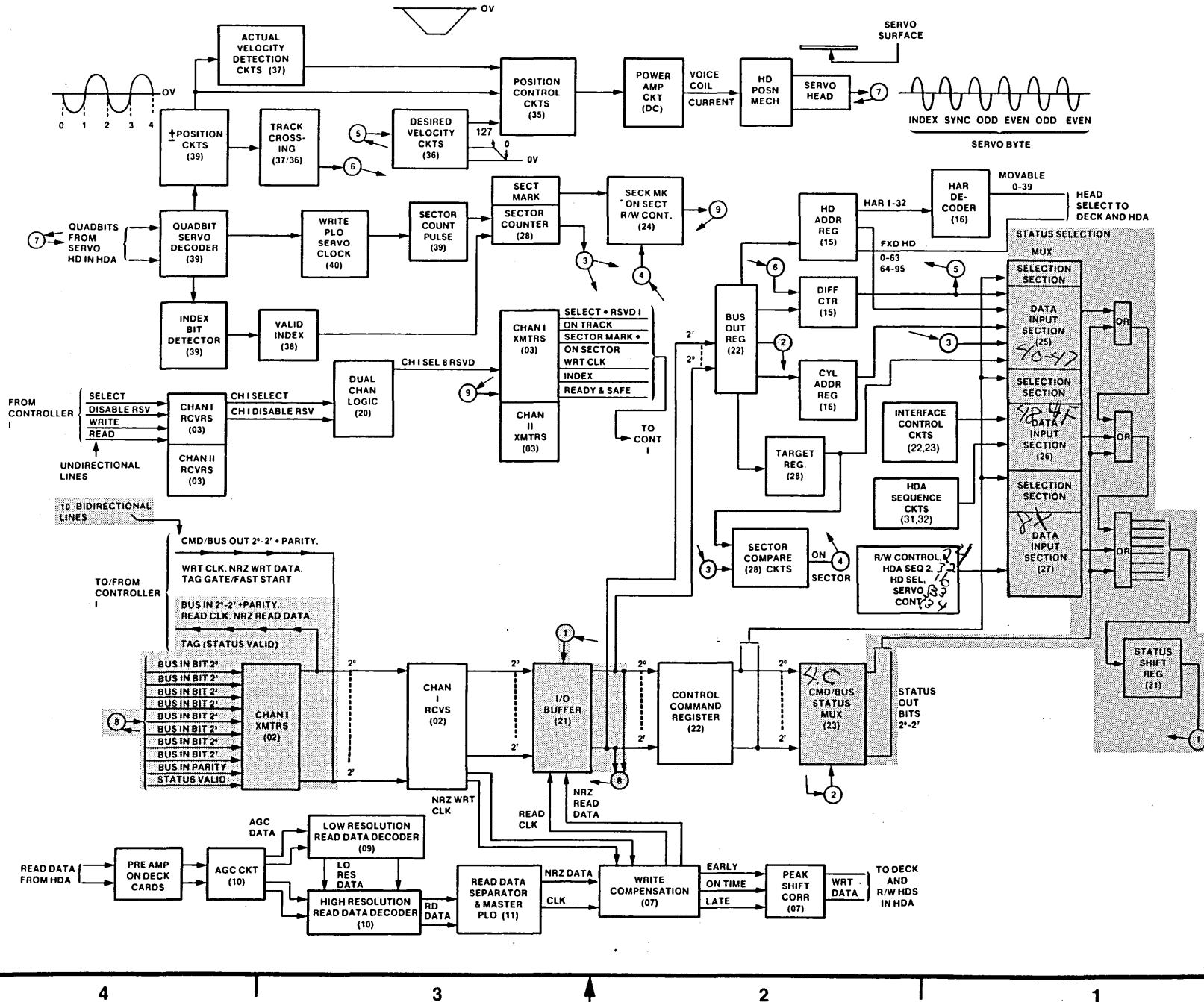
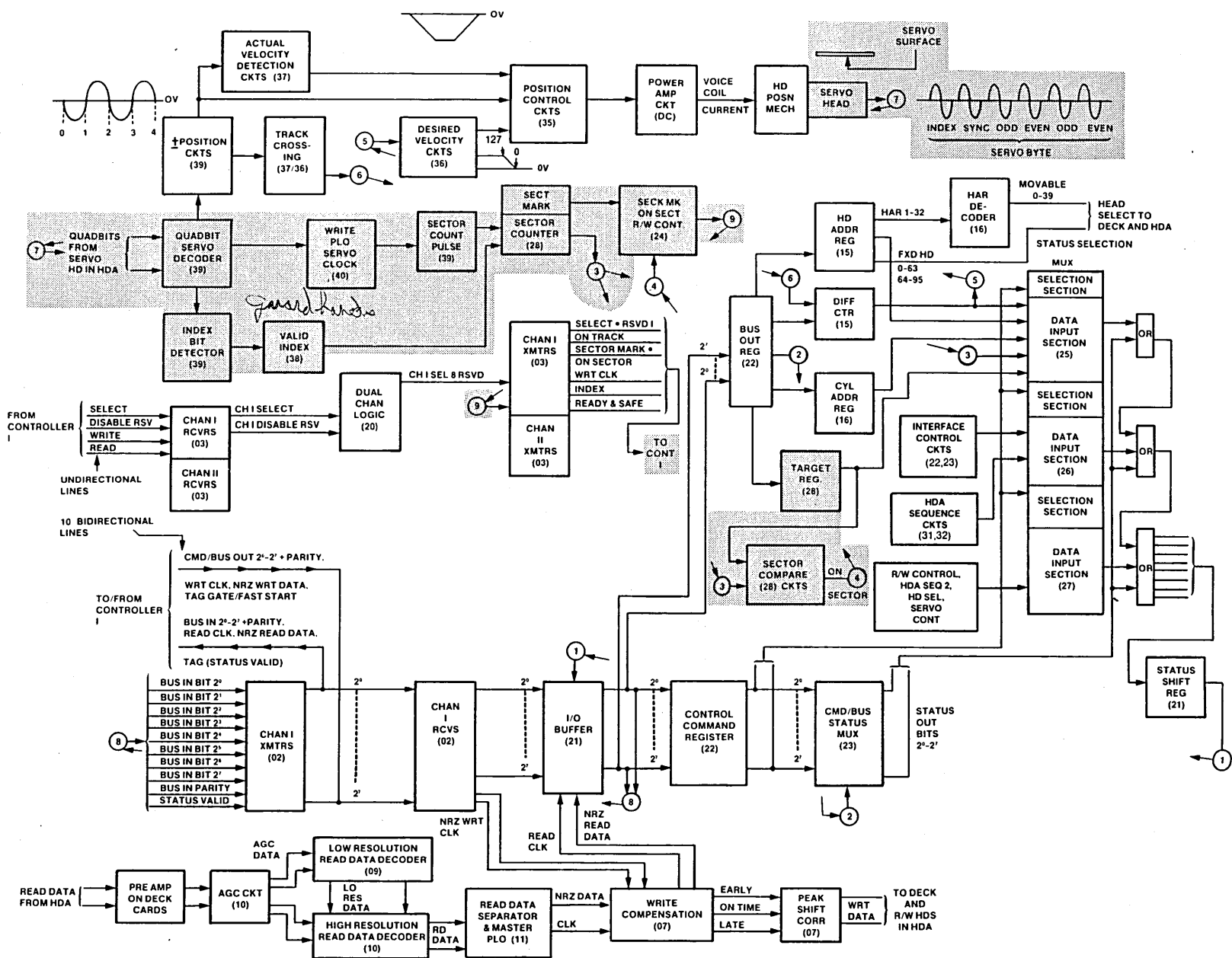


Figure 3-43. Detailed Block Diagram - On Sector



D

—

C

→

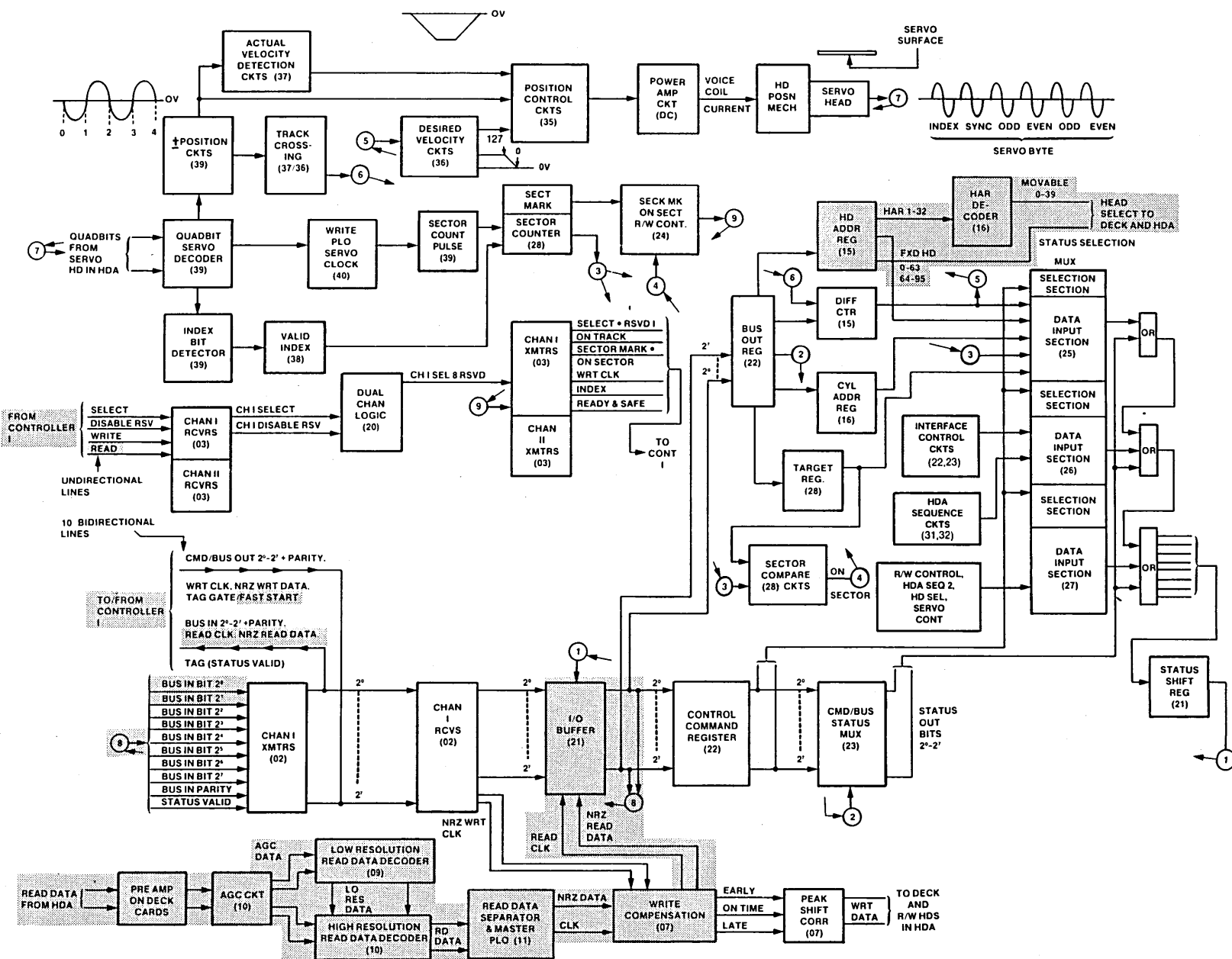
B

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A



Figure 3-45. Detailed Block Diagram - Read



LEARNING ACTIVITY 3-L. EXERCISE: DETAILED BLOCK DIAGRAM REVIEW

This activity reviews the Fixed Module Drive Detailed Block Diagram. After completing the exercise, check your answers with those given at the end of this Learning Activity.

OBJECTIVE

- You will be able to list the major functional areas of the 885 Fixed Module Drive detailed block diagram and describe the purpose of each area.

Directions: After reading each of the following statements, fill in the blank(s) with a word or words to complete the statement and make it true.

1. The Interface signals received by the channel II RCVR board at location 03 are select, disable reserve, write, and read.
2. The Index signal is sent to the controller by the logic board at location 03.
3. The device-Unique ID switches are on the logic board at location 20.
4. The dual channel logic board at location 20 is (is/is not) present in a single access device.
5. The receivers and transmitters for both controller I and II uni-directional lines are on the logic board at location 7.
6. The receivers and transmitters for controller II's bidirectional lines are on the logic board at location 7.
7. The purpose of the logic board at location 21 is to allow either channel I or the channel II CMD/ bus-out data to the command and bus-out registers.
8. 4X and 8X commands are loaded into the Control Command register at board location 22.
9. The second Tag Gate signal loads the Bus out at board location 22.

CYBER Fixed Module Drive
Learning Activity 3-L

10. Two CMD/bus-out sequences are required to load both the upper and lower cylinder register at board location 16.
11. The selected status goes through the status shift register then to the I/O buffer at location 21.
12. The cylinder address is enabled through the status mux logic board at location 25.
13. The board at location 25 will be enabled when the control command register contains a 40 through 47 command.
14. The transmitters for the status words sent to controller I are on the logic board at location 2.
15. The CMD/bus status mux is used by the 4C command.
16. When at the home position, the servo head is at the outer edge of outer guard band 2.
17. A power-on rezero seek operation moves the heads from the home position to cylinder 0.
18. A power-off go home operation moves the heads from any cylinder address to the home position.
19. The digital to analog converter for the servo logic is on the logic board at location 36.
20. The pot to adjust the servo speed is on the logic board at location 39.
21. The head positioner mechanism block represents the magnet, voice coil, and the carriage.
22. The servo head reads (reads/writes) the servo disk surface.
23. The difference counter contains the difference between where the carriage is now and where it will move to.
24. The D to A converter output is maximum when there is more than 127 tracks to go in the positioning operation.

CYBER Fixed Module Drive
Learning Activity 3-L

25. The power amp circuit is physically located in the DC power supply.
26. The Plus and Minus Position signal crosses the zero volt reference when the servo head crosses a track.
27. The difference counter decrements (increments/decrements) as each track is crossed.
28. The faster the carriage moves, the greater (greater/less) the analog voltage from the actual velocity detection circuit at board location 37.
29. The polarity of the analog voltage for a forward or reverse is determined by the forward and reverse gates on the logic board at location 35.
30. The circuit that generates the index mark is on the board at location 38.
31. The sector compare circuit on the board at location 28 compares the count in the sector counter with the contents of the target register.
32. Before a read or write operation can begin, one head must be selected.
33. The movable head select is sent to the deck logic by the board at location HAR Decoder-16.
34. The write data from the controller is in the NRZ (MFM/NRZ) format.
35. The write compensation logic on the board at location 7 writes the data pulse earlier, on time, or late to compensate for the peak shift distortion.
36. The write data is sent to the deck logic by the board at location Peak shift correction 07.
37. Before a read operation may begin the controller must send a control select command.
38. The read data path is through the preamps on the deck logic cards to the AAC 10 to the high and low resolution read data decoders.

CYBER Fixed Module Drive
Learning Activity 3-L

39. The read data separation logic on the board at location 11 puts the read data into the NRZ (MFM/NRZ) format.
40. The read data and clock passes through the write compensation board, to the I/O Buffer - 21, to the channel transmitters.
41. The transmitters for sending the read data and clock to the channel II controller are on the logic board at location 04.

CYBER Fixed Module Drive
Learning Activity 3-L

The answers to this learning activity are on the following page.

CYBER Fixed Module Drive
Learning Activity 3-L

ANSWERS TO LEARNING ACTIVITY 3-L

- | | |
|--|---|
| 1. Select, disable reserve,
write, read | 21. voice coil |
| 2. three | 22. reads |
| 3. twenty | 23. now, will |
| 4. is | 24. one-hundred twenty-seven |
| 5. three | 25. DC |
| 6. four | 26. track |
| 7. twenty-one, I/O Buffer | 27. decrements |
| 8. control command | 28. greater |
| 9. bus-out register | 29. thirty-five, position
control circuits |
| 10. two | 30. thirty-eight |
| 11. status shift | 31. sector counter, target |
| 12. twenty-five | 32. one |
| 13. forty-seven | 33. sixteen, HAR decoder |
| 14. two | 34. NRZ |
| 15. 4C or set diagnostic | 35. on time, later |
| 16. home | 36. seven |
| 17. zero | 37. controller |
| 18. go home | 38. AGC circuit on board at
location 10 |
| 19. thirty-six, desired
velocity circuits | 39. NRZ |
| 20. thirty-nine, feedback
signal generator circuits | 40. I/O Buffer |
| | 41. four |

LEARNING ACTIVITY 3-M. AUDIOTAPE: BASIC POWER SEQUENCE

This activity describes the basic power sequence diagrams of the FMD power supply.

OBJECTIVE

- You will be able to list the steps in the 885 Fixed Module Drive basic power sequence in proper order.

Figures 3-46 through 3-52 contain the basic power sequence diagrams. There are three types of diagrams. Figure 3-46 is the DC power supply. Figures 3-47, 3-48, and 3-49 are the power-on diagrams. Figures 3-50, 3-51, and 3-52 are the power complete diagrams. The tape will describe the highlighted areas on each figure. You may stop the tape at any time to take notes or go over some topics again.

Load the audiotape Basic Power Sequence (75445256) into your cassette player and turn to figure 3-46.

NOTE

Appendix D contains the script of this audiotape.

STUDENT NOTES

Figure 3-46. DC Power Supply

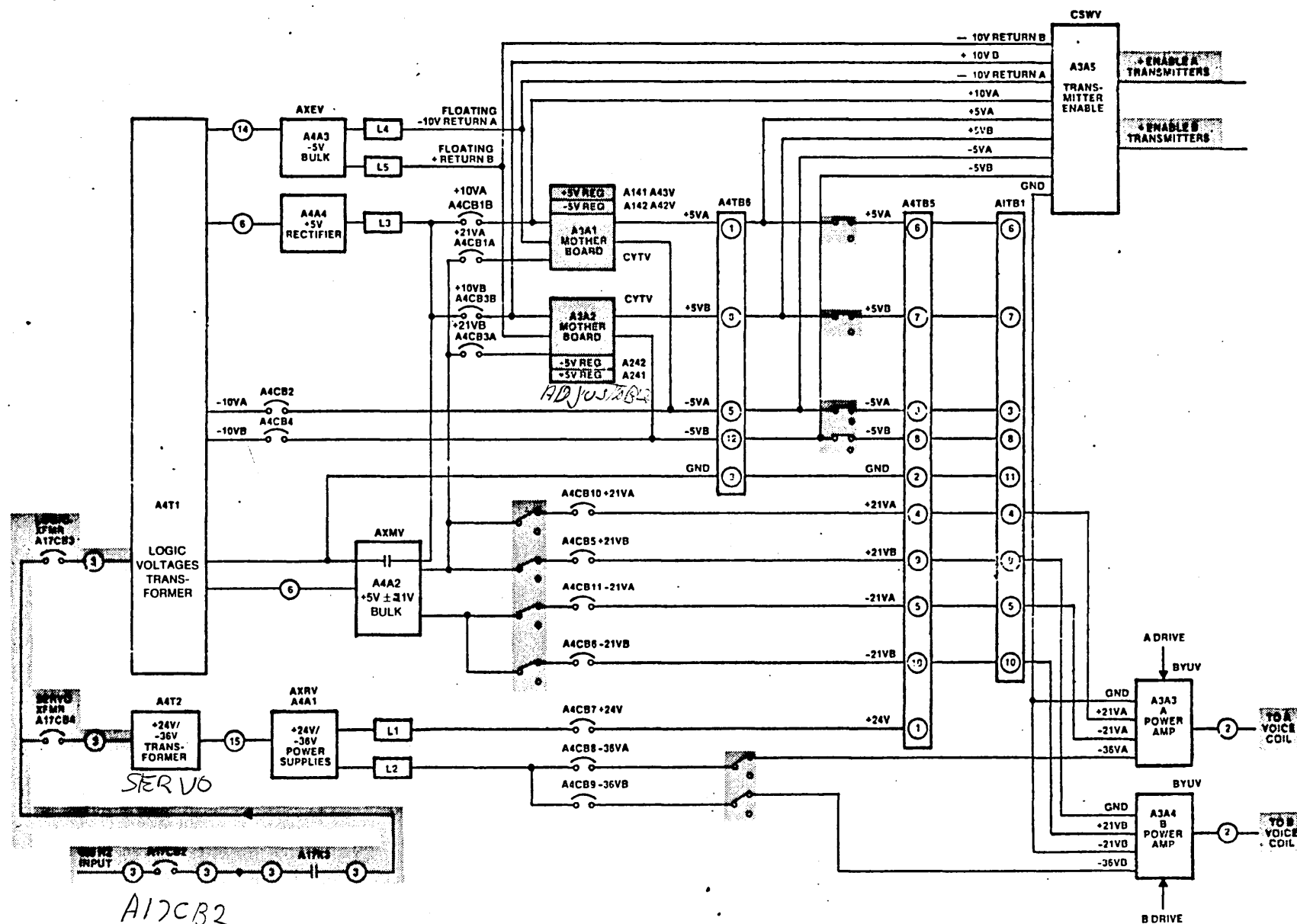


Figure 3-47. Power On-1

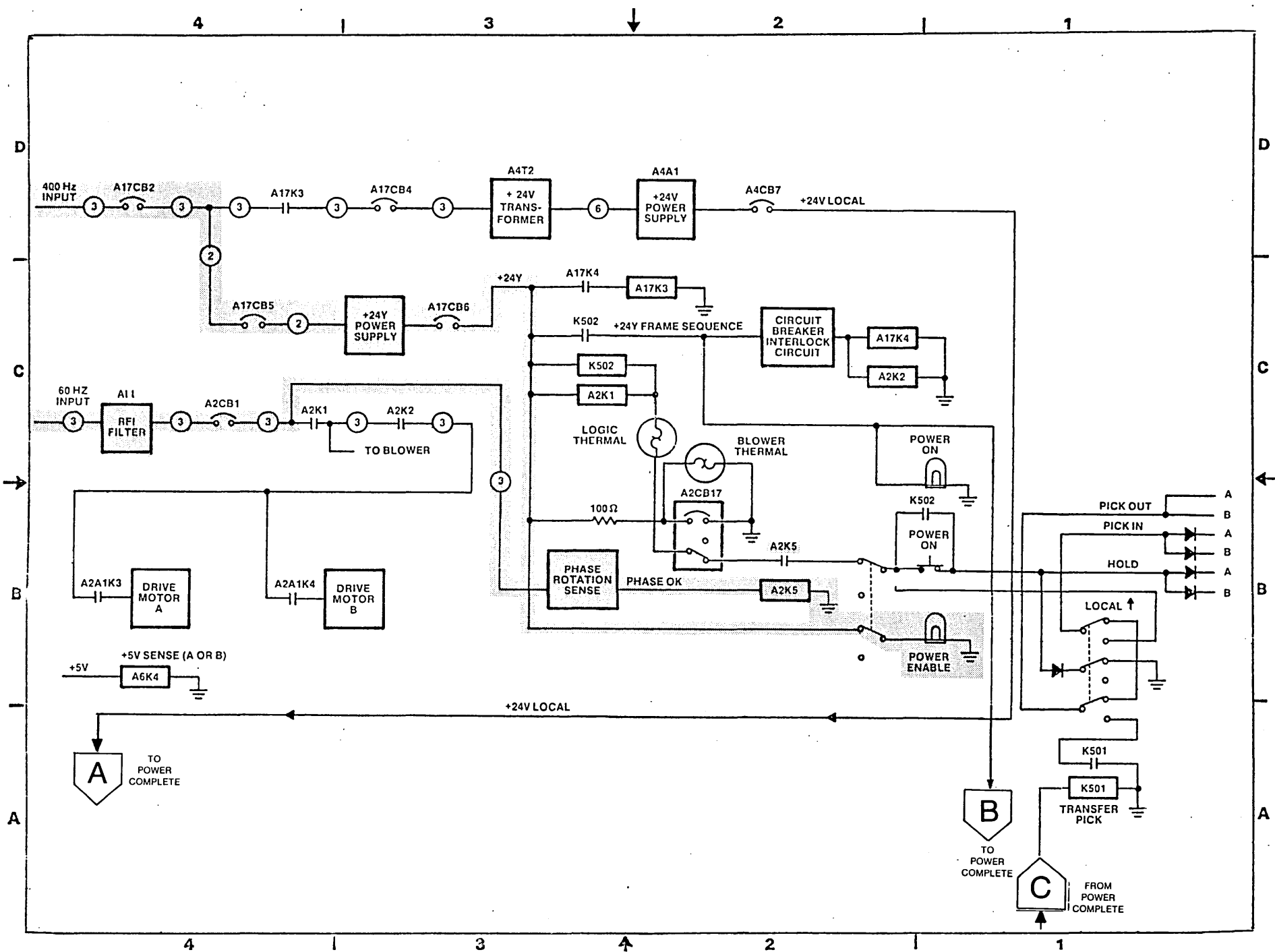


Figure 3-48. Power On-2

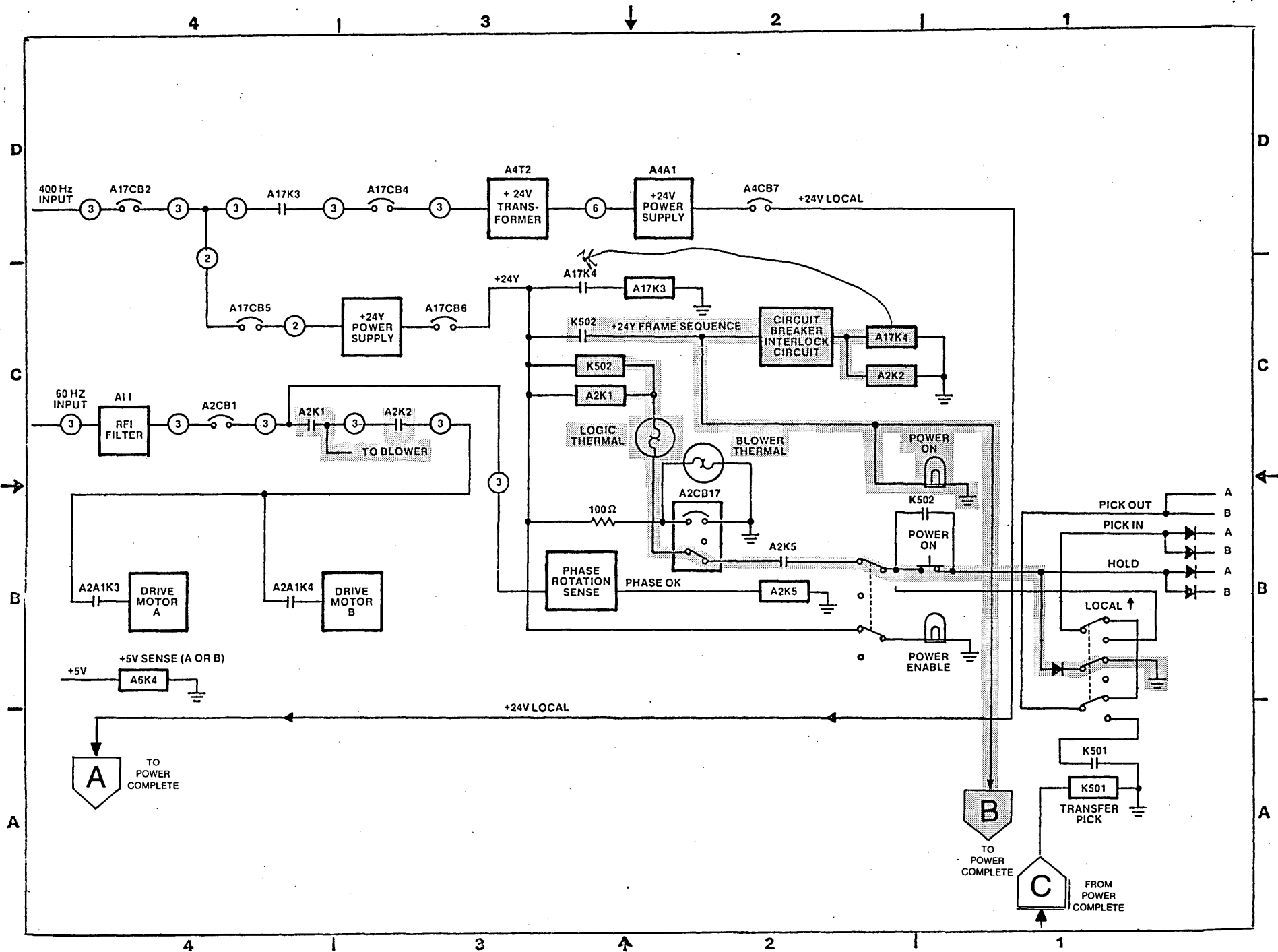


Figure 3-49. Power On-3

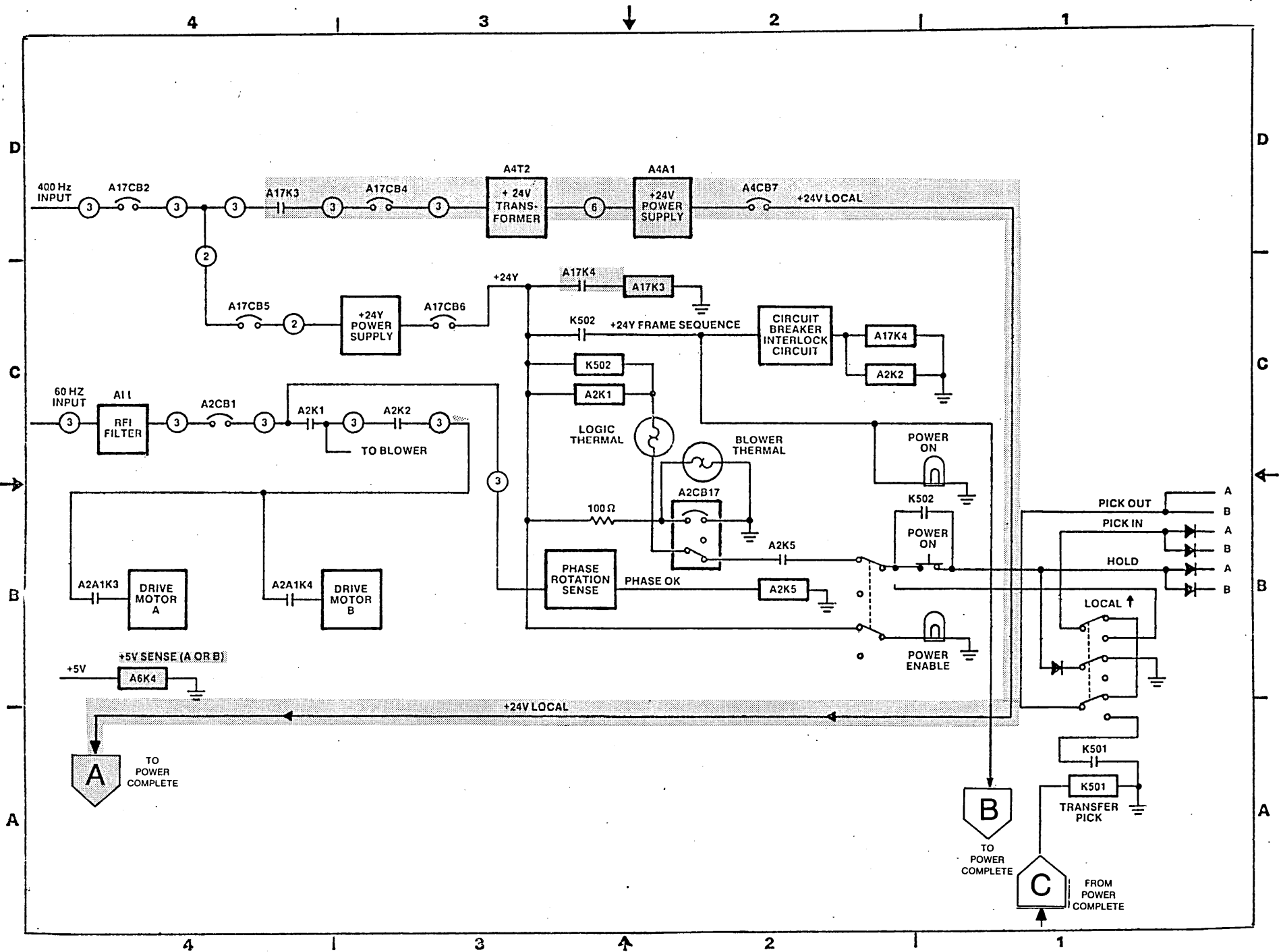


Figure 3-50. Power Complete-1

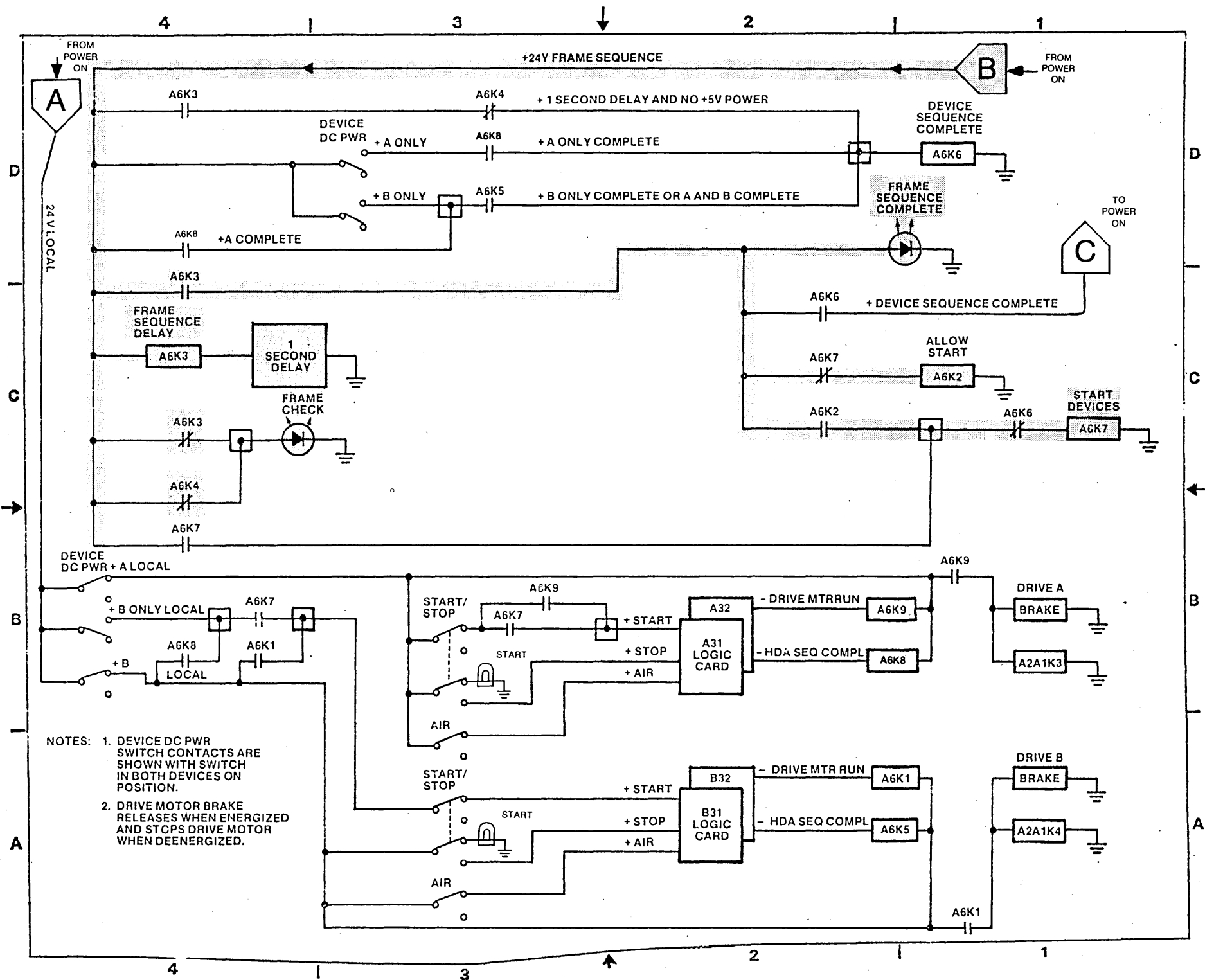


Figure 3-51. Power Complete-2

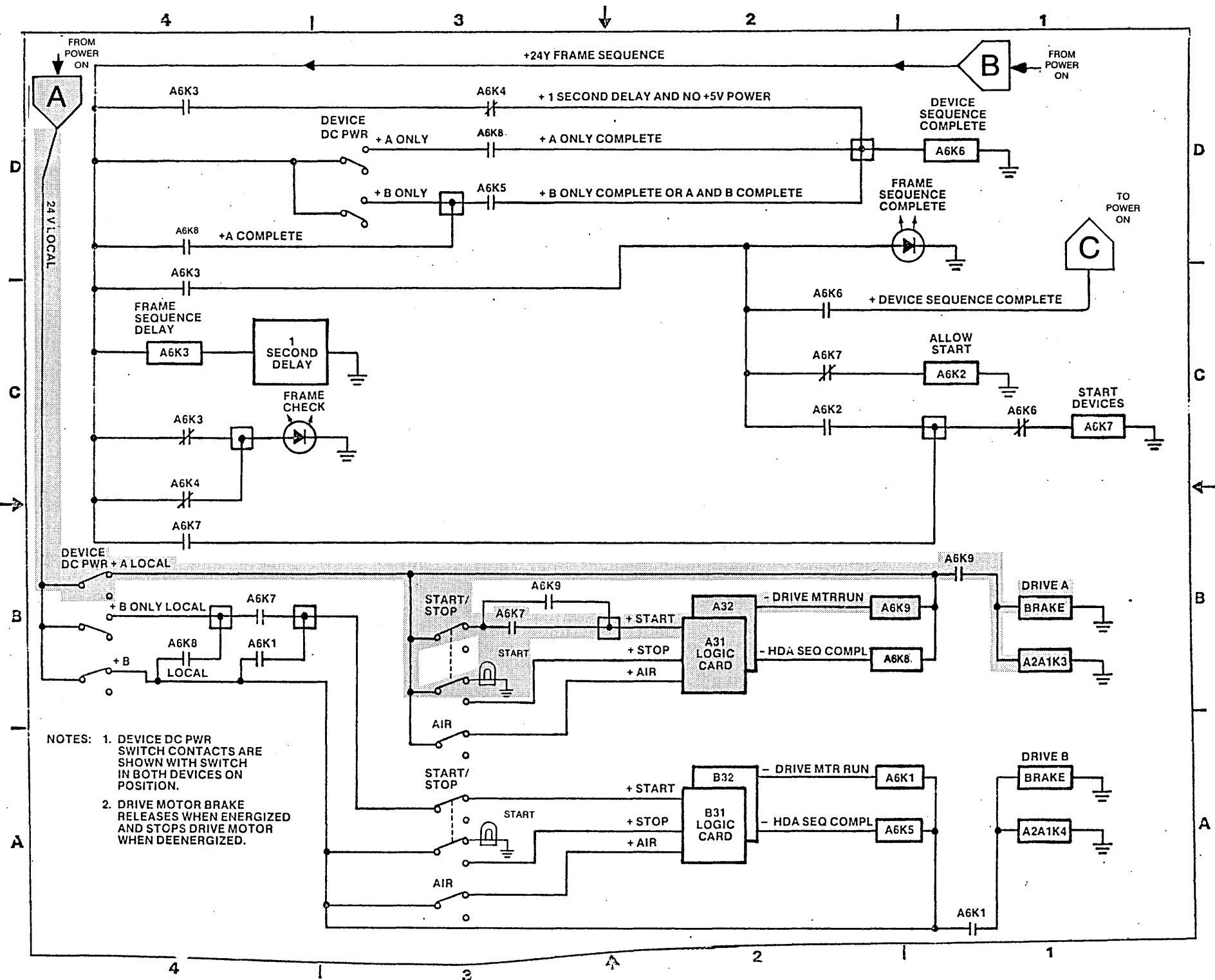
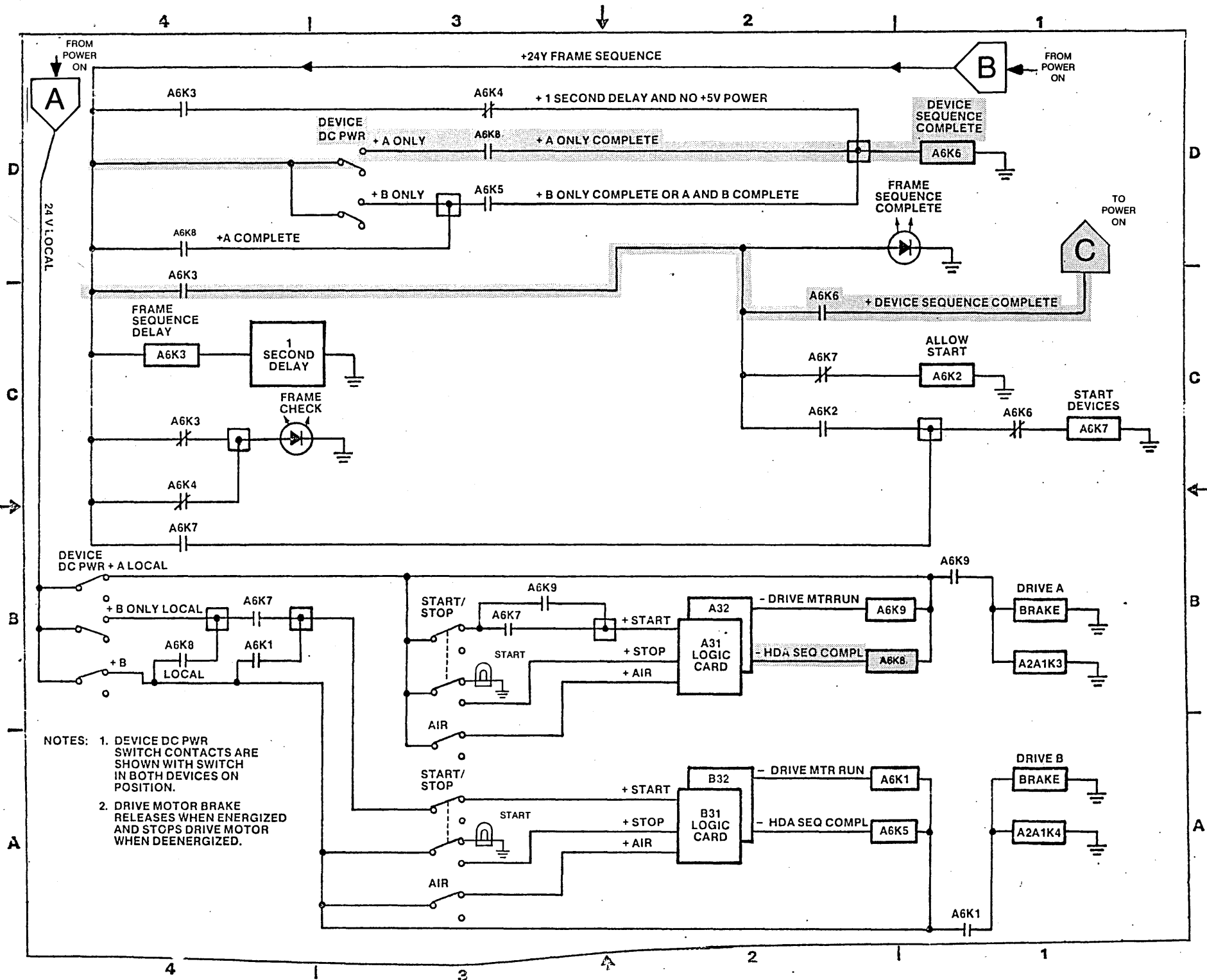


Figure 3-52. Power Complete-3



LEARNING ACTIVITY 3-N. EXERCISE: BASIC POWER SEQUENCE REVIEW

This activity reviews the fixed module drive basic power sequence diagrams. After completing the exercise, check your answers with those given at the end of this learning activity.

OBJECTIVE

- You will be able to list the steps in the 885 Fixed Module Drive basic power sequence in proper order.

Directions: After reading each of the following statements, fill in the blank(s) with a word or words to complete the statement and make it true.

1. The DC power supply has a power amp for each (one/each) device.
2. The adjustable 5-volt regulator for device A is on mother board A3 A1.
3. The 3Ø 400 Hz signal is the input to the logic and servo transformer.
4. The circuit breaker for -36 volts for device A is A4CB 8.

Directions: The following questions refer to the power-on diagrams.

5. The 400-Hz input goes to the +24Y power supply in the AC (AC/DC) power supply.
6. The phase rotational sense circuit monitors the 60 (60/400) Hz input.
7. The power enable indication is lit by 24 volts when the power enable switch is on (on/off).
8. The blower will be turned on after relay A2 K1 is energized.
9. The power on indicator lights immediately after relay K502 energizes.

CYBER Fixed Module Drive
Learning Activity 3-N

10. +24 volts local is generated by the +24 volt transformer and power supply after relay A12 K3 energizes.

11. Relay A6K4 is energized by the +5 V sense.

Directions: The following questions refer to the power complete diagrams.

12. The frame check LED goes off after relays A6K3 and A6K4 energize (energize/de-energize).

13. The frame sequence complete LED is turned on after relay A6 K3 energizes.

14. The device DC power **switch** is in the B-only position. The Start signal is sent to the B31 logic card after relay _____ energizes.

15. The device DC power switch is in the both-devices position. The Start signal is sent to the B31 logic card after relay A6 K7 energizes.

16. The relay that energizes to enable 60 Hz to the drive motor for device B is relay A2 A1 K4.

17. The brake for device A is released (energized/released) after relay A6K9 energizes.

18. The device DC power switch is in the A-only position. The device sequence complete relay, A6 K6, is energized after relay A6 K8 energizes.

CYBER Fixed Module Drive
Learning Activity 3-N

Directions: The events of a local power-up of device A are listed on the right. Use the left column blanks to arrange the events in chronological order. All CBs are closed and power-on, power-enable, and start switches are on.

- | | |
|-----------------|--|
| <u>1 D</u> 19. | <u>8</u> a. ✓ Energize A6K7 |
| <u>2 F</u> 20. | <u>5</u> b. ✓ Energize A6K3 |
| <u>3 K</u> 21. | <u>9</u> c. ✓ Generate drive motor run |
| <u>4 G</u> 22. | <u>11</u> d. ✓ Generate phase OK |
| <u>5 B</u> 23. | <u>12</u> e. Generate device sequence complete |
| <u>6 J</u> 24. | <u>2</u> f. ✓ Energize A2K5 |
| <u>7 L</u> 25. | <u>4</u> g. ✓ 400 Hz to DC power supply |
| <u>8 A</u> 26. | <u>11</u> h. ✓ Energize A6K8 |
| <u>9 C</u> 27. | <u>10</u> i. ✓ Energize A2A1K3 |
| <u>10 I</u> 28. | <u>6</u> j. ✓ Generate frame sequence complete |
| <u>11 h</u> 29. | <u>3</u> k. ✓ Turn on blower |
| <u>12 e</u> 30. | <u>7</u> l. ✓ Energize A6K2 |

CYBER Fixed Module Drive
Learning Activity 3-N

ANSWERS TO LEARNING ACTIVITY 3-N

- | | |
|--|--------------|
| 1. each | 15. A6K8 |
| 2. A1 | 16. A2A1K4 |
| 3. four hundred | 17. released |
| 4. eight | 18. K6, K8 |
| 5. AC | 19. d |
| 6. sixty | 20. f |
| 7. +24Y, on | 21. k |
| 8. K1 | 22. g |
| 9. K502 | 23. b |
| 10. A17K3 | 24. j |
| 11. +5 volt sense circuit
for device A or B | 25. l |
| 12. energize | 26. a |
| 13. A6K3 | 27. c |
| 14. A6K7 | 28. i |
| | 29. h |
| | 30. e |

POST TEST

When you have completed the learning activities assigned for module 3, sign on to the PLATO terminal and take the module 3 test.

You may use your student manual and your reference manuals during the test. Be sure to take them with you to the PLATO terminal.

Depending on the results of the test, you will be told either to review some of the activities in this module or to go on to module 4.

MODULE 4

INTRODUCTION TO THE 7155 CONTROLLER

This module will acquaint you with the components and theory of the 7155-1 (FA211-A) controller. You will learn the location of components through locator diagrams and how the logic is organized through block diagrams.

NOTE: Newer controllers have revised logic modules, logic module locations, LED locations, power supplies, and options. This course is based on the 7155-1 (FA211-A). Always use your site manuals as reference for the equipment you are maintaining.

PRETEST

To begin this module, sign on to the PLATO terminal and read the objectives. If you feel you might be able to meet some of the objectives, take the module test. After evaluating the results of your test, PLM will assign the learning activities that relate to the objectives you did not meet. If you do not wish to take the test first, ask for an assignment.

LEARNING ACTIVITIES

In the assigned column below put a checkmark by each activity assigned to you by PLM. Proceed through the assigned activities and check off each activity as you complete it. You may choose to do all of the activities more than once.

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	4-A	Text Reading: Controller Components. This activity describes the features, physical components, and power sequence interface of the 7155 controller.	4-3
_____	_____	4-B	Exercise: Controller Components Review. This activity reinforces learning activity 4A.	4-18

CYBER Fixed Module Drive
Module 4

<u>Assigned</u>	<u>Completed</u>	<u>Activity</u>	<u>Description</u>	<u>Page</u>
_____	_____	4-C	Text Reading: Functional Elements. This activity describes the functional elements, PP interface signals, and defines the function, parameter, data and status words of the 7155 controller.	4-21
_____	_____	4-D	Exercise: Functional Elements Review. This activity reinforces learning activity 4-C.	4-30
_____	_____	4-E	Text Reading: Status Words. This activity describes the general and detailed status words for the 885 FMD and 844 disk drives on the 7155 controller.	4-33
_____	_____	4-F	Exercise: Status Words Review. This activity reinforces learning activity 4-E.	4-39
_____	_____	4-G	Audiotape: 7155 Block Diagram. This activity describes the 7155 controller block diagram.	4-41
_____	_____	4-H	Exercise: 7155 Block Diagram Review. This activity reinforces learning activity 4-G.	4-48

LEARNING ACTIVITY 4-A. TEXT READING: CONTROLLER COMPONENTS

This activity describes the features, physical components, and power sequence interface of the 7155 controller.

OBJECTIVE

- You will be able to describe the function of the major components of the 7155 controller.

The 7155 controller, equipment number FA211-A, contains one access to a PP data channel and accesses for four BZ703 (885) fixed module drives (FMD). Each drive has two spindles that must be addressed as separate devices. Three FV662-A channel access options can be added to the controller. Each of these options provides an access for another PP channel. The FV670-A/B 844 option provides an access for eight BR308/BR312 (844) disk storage units. The FV671-A/B four FMD option adds four FMD accesses (eight devices) to the controller.

CYBER Fixed Module Drive
Learning Activity 4-A

The 7155 controller components consist of a switch panel, two rows of logic, a blower assembly for cooling the logic, a power distribution panel, I/O connector panels for the PP, 844, 885 FMD, and the 885 power sequence interface (see figure 4-1).

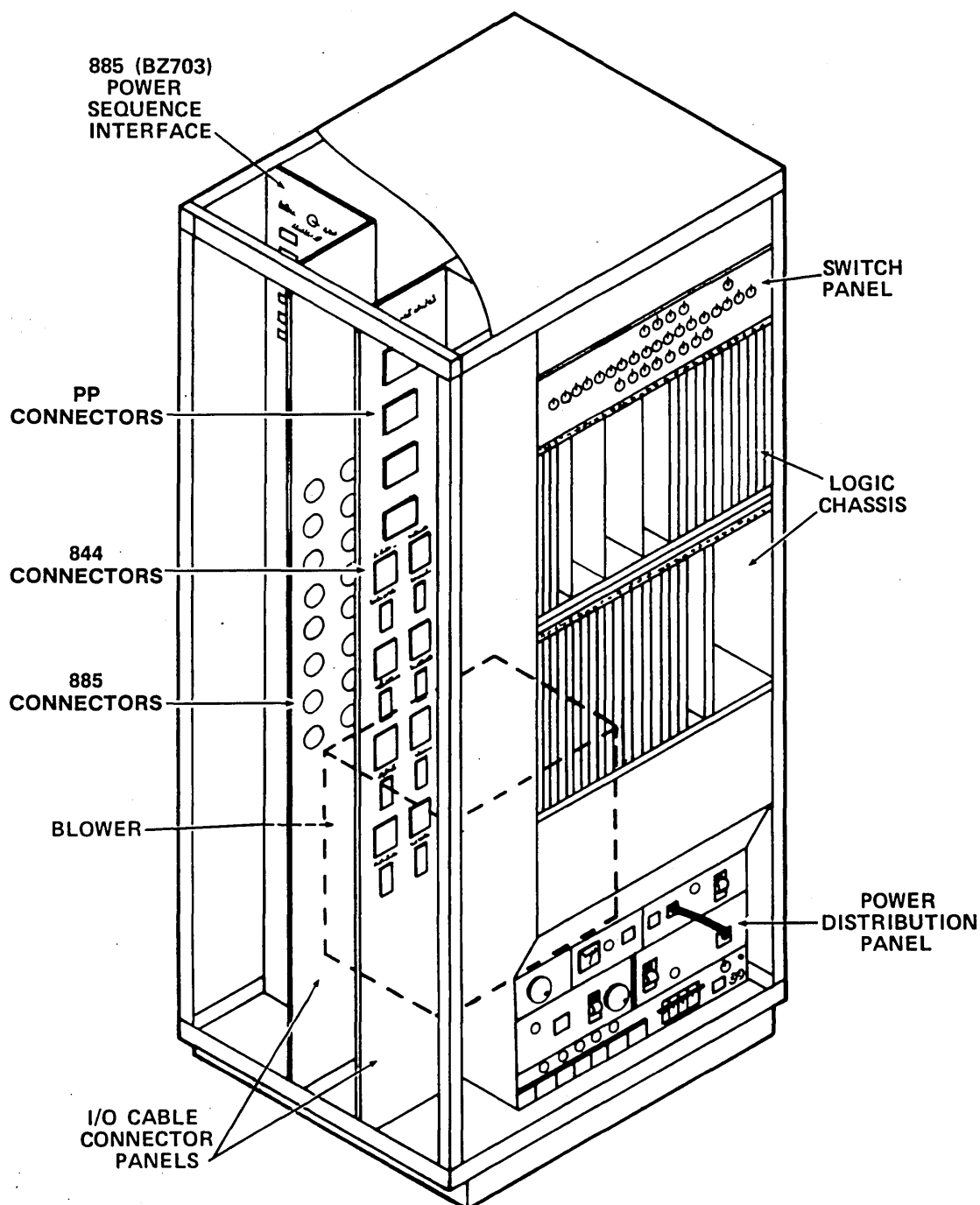


Figure 4-1. Controller Components

CYBER Fixed Module Drive
Learning Activity 4-A

Figure 4-2 shows the location of the controller power on indicator and operator switches. Table 4-1 describes the functions of the switches and indicator.

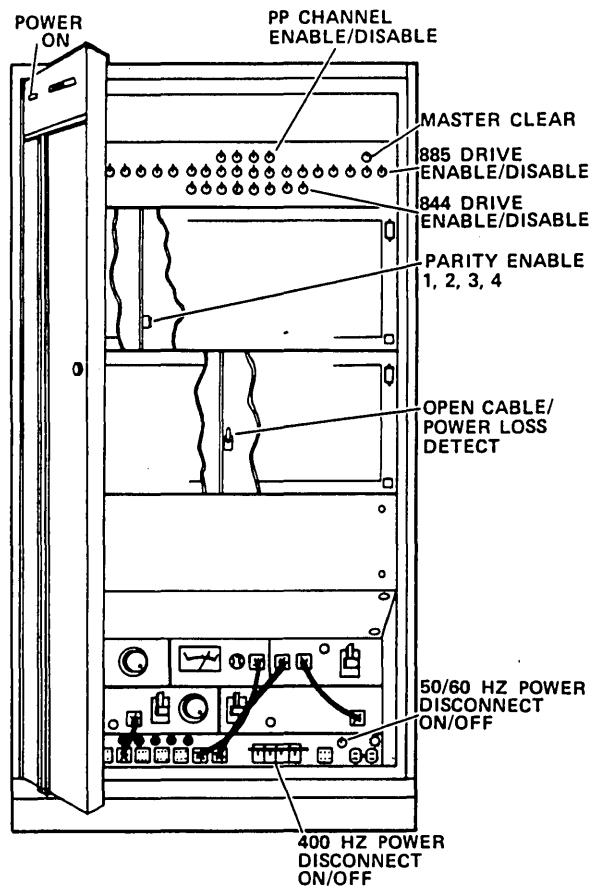


Figure 4-2. Controller Switch/Indicator Locations

CYBER Fixed Module Drive
Learning Activity 4-A

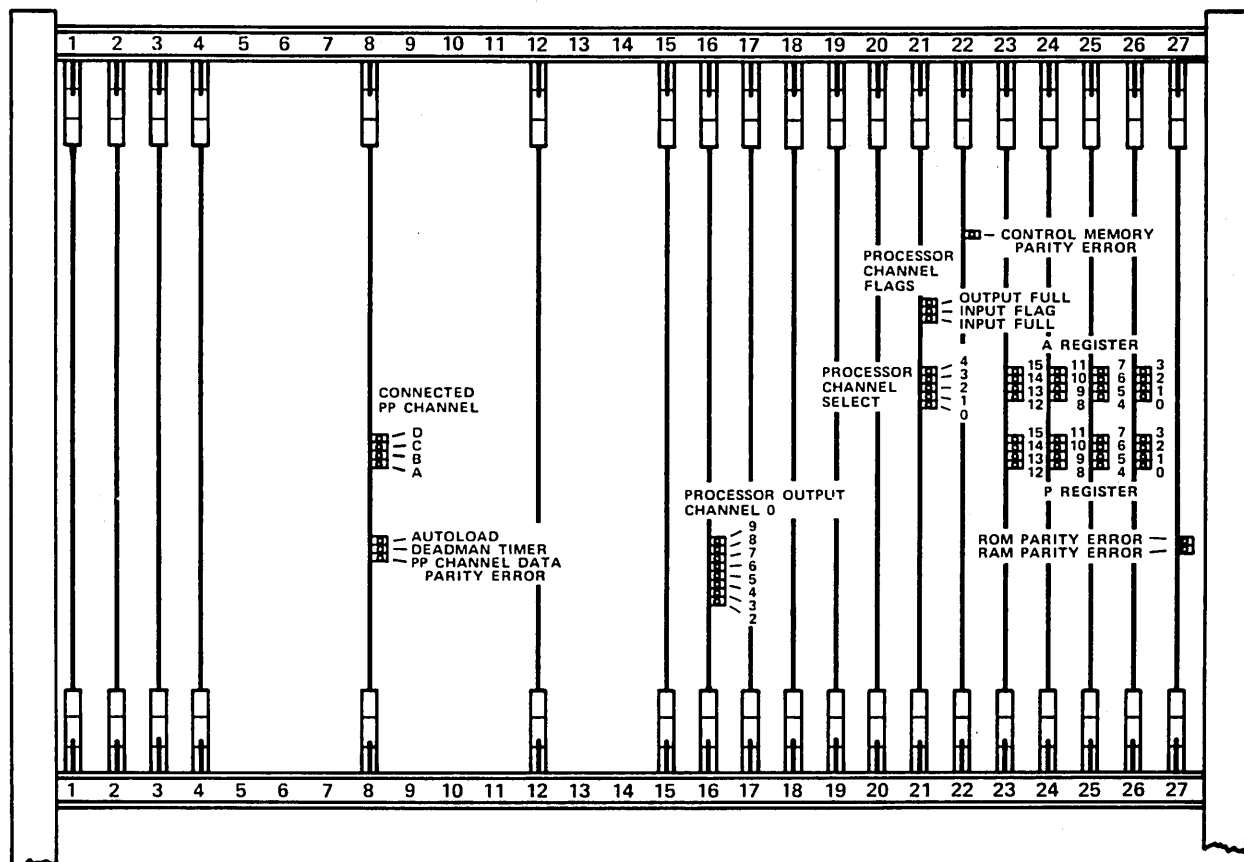
TABLE 4-1. CONTROLLER SWITCHES/INDICATOR

Name	Type	Function
POWER ON	Indicator	Lights when power is applied to controller.
PP CHANNEL ENABLE/ DISABLE	Four toggle switches	Enables/disables communication between controller and PP channel attached to access associated with switch.
MASTER CLEAR	Pushbutton switch	Clears controller logic and connected access and forces processor memory address to 20 000 ₈ .
885 DRIVE ENABLE/ DISABLE	Sixteen toggle switches	Enables/disables communication between controller and 885 drive attached to connector associated with switch.
844 DRIVE ENABLE/ DISABLE	Eight toggle switches	Enables/disables communication between controller and 844 drive attached to connectors associated with switch.
50/60 HZ POWER DISCONNECT ON/OFF	Toggle switch	ON: Applies power to blower. OFF: Removes power from blower.
400 HZ POWER DISCONNECT ON/OFF	Toggle switch	ON: Applies power to controller logic. OFF: Removes power from controller logic.
1,2,3,4 ON/OFF	Four switches (at chassis location A08)	ON: Enables parity for the respective PP access. 1 = access A, 2 = access B, 3 = access C, 4 = access D. OFF: Disables parity.
PROTECTED/ DISABLE	Toggle switch (at chassis location B13)	Enables open cable/power loss detect circuit. Disables this circuit. NOTE: Put in disable (down) position when running voltage margins.

CYBER Fixed Module Drive Learning Activity 4-A

There are two rows of 60-pak ECL (emitter coupled logic) in the logic chassis. The top row is the A row and the bottom row is the B row. The A row has light emitting diodes (LEDs) mounted on the front edge of nine of the logic boards.

The A row of logic and the LEDs are shown in figure 4-3. The LEDs are useful in fault isolation. In a later learning activity, you will use the diagnostics and LEDs to isolate failing logic boards.



NOTES:

1. LED ON INDICATES 1, LED OFF INDICATES 0.
2. A NUMBER NEXT TO A LED INDICATES THE POWER OF 2 REPRESENTED BY THE LED.

Figure 4-3. LED Locations

CYBER Fixed Module Drive
Learning Activity 4-A

The following paragraphs describe the function of each LED when lit.

- Connected PP Channel A, B, C, and D indicate which PP channel is connected in the controller hardware.
- Autoload indicates that the connected PP has sent an autoload function. A master clear or another function clears the LED.
- Deadman Timer indicates that a CDC CYBER channel timeout occurred.
- PP channel data parity error indicates that the controller detected a parity error (even parity) on a word sent by the connected PP. Parity must be enabled to light this indicator.
- Processor output channel 0, 2 through 9 reflect the contents of NOC0/2-9.
- Output full, input flag, input full indicate that the output full, input flag, or input full signal is present on the selected processor channel.
- Processor channel select 0, 1, 2, 3, and 4 indicate which channel has been selected by the processor. The number of the selected channel, 0 through 16, corresponds to the octal code shown by the indicators.
- Control memory parity error indicates a parity error (even parity) was detected in one or more of the 12-bit bytes of the 60-bit word. Master clear clears this condition.
- A register indicates the contents of the accumulator register during a halt instruction.
- P register indicates the current program address in the processor. The P register equals 21BF when the processor is in its idle loop.
- ROM parity error, and RAM parity error indicate that the processor has halted because of a parity error (even parity) in a word read from the program ROM, program RAM, or buffer RAM.

CYBER Fixed Module Drive Learning Activity 4-A

The two rows of ECL 60-pak are shown by the card placement chart in figure 4-4. Each card or board location is labeled by board function. For example, the board at location A12 is the error correction board.

Each board location is labeled with a two-character code to designate card type. For example, the board at location B17 is card type AM.

Each board location is also labeled with a Control Data part number. For example the board at location A08 is Control Data part number 22936328.

A

27	PROGRAM ROM, PARITY 22939170	TYPE: AK
26	4 BIT SLICE PROCESSOR 22932929	TYPE: AJ
25	4 BIT SLICE PROCESSOR 22932929	TYPE: AJ
24	4 BIT SLICE PROCESSOR 22932929	TYPE: AJ
23	4 BIT SLICE PROCESSOR 22932929	TYPE: AJ
22	CONTROL MEMORY 52787155	TYPE: AH
21	CHANNEL CONTROL 11896398	TYPE: AG
20	PROCESSOR CHANNELS 22934533	TYPE: AF
19	PROCESSOR CHANNELS 22934533	TYPE: AF
18	PROCESSOR CHANNELS 22934533	TYPE: AF
17	PROCESSOR CHANNELS 22934533	TYPE: AF
16	SPECIAL CYBER CHANNEL 11896752	TYPE: AE
15	BUFFER CONTROL 11897694	TYPE: AD
14		
13		
12	ERROR CORRECTION 11897798	TYPE: AC
11		
10		
9		
8	CYBER CHANNEL MUX 22936328	TYPE: AB
7		
6		
5		
4	CHANNEL R/T D (FV662-A) 10358598	TYPE: AA
3	CHANNEL R/T C (FV662-A) 10358598	TYPE: AA
2	CHANNEL R/T B (FV662-A) 10358598	TYPE: AA
1	CHANNEL R/T A 10358598	TYPE: AA

A

B

27		
26		
25		
24		
23		
22	DATA PATH CONTROL 11899014	TYPE: AT
21	BUFFER TO DATA PATH CONTROL 11899010	TYPE: AS
20	READ/WRITE DATA PATH 11896751	TYPE: AR
19	READ/WRITE DATA PATH 11896751	TYPE: AR
18		
17	DRIVE INTERFACE CONTROL (FV671-A/B) 22938728	TYPE: AM
16	DRIVE INTERFACE BUS (FV671-A/B) 22939189	TYPE: AL
15	DRIVE INTERFACE BUS (FV671-A/B) 22939189	TYPE: AL
14	DRIVE INTERFACE BUS (FV671-A/B) 22939189	TYPE: AL
13	844 INTERFACE CONTROL 11899080	TYPE: AP
12	844 INTERFACE 8:1 (FV670-A/B) 11899094	TYPE: AN
11	844 INTERFACE 8:1 (FV670-A/B) 11899094	TYPE: AN
10	844 INTERFACE 8:1 (FV670-A/B) 11899094	TYPE: AN
9	844 INTERFACE 8:1 (FV670-A/B) 11899094	TYPE: AN
8	844 INTERFACE 8:1 (FV670-A/B) 11899094	TYPE: AN
7	844 INTERFACE 8:1 (FV670-A/B) 11899094	TYPE: AN
6	844 INTERFACE 8:1 (FV670-A/B) 11899094	TYPE: AN
5	844 INTERFACE 8:1 (FV670-A/B) 11899094	TYPE: AN
4	DRIVE INTERFACE CONTROL 22938728	TYPE: AM
3	DRIVE INTERFACE BUS 22939189	TYPE: AL
2	DRIVE INTERFACE BUS 22939189	TYPE: AL
1	DRIVE INTERFACE BUS 22939189	TYPE: AL

B

Figure 4-4. Chassis Map

CYBER Fixed Module Drive
Learning Activity 4-A

Figure 4-5 shows the power supply area at the base of the controller cabinet.

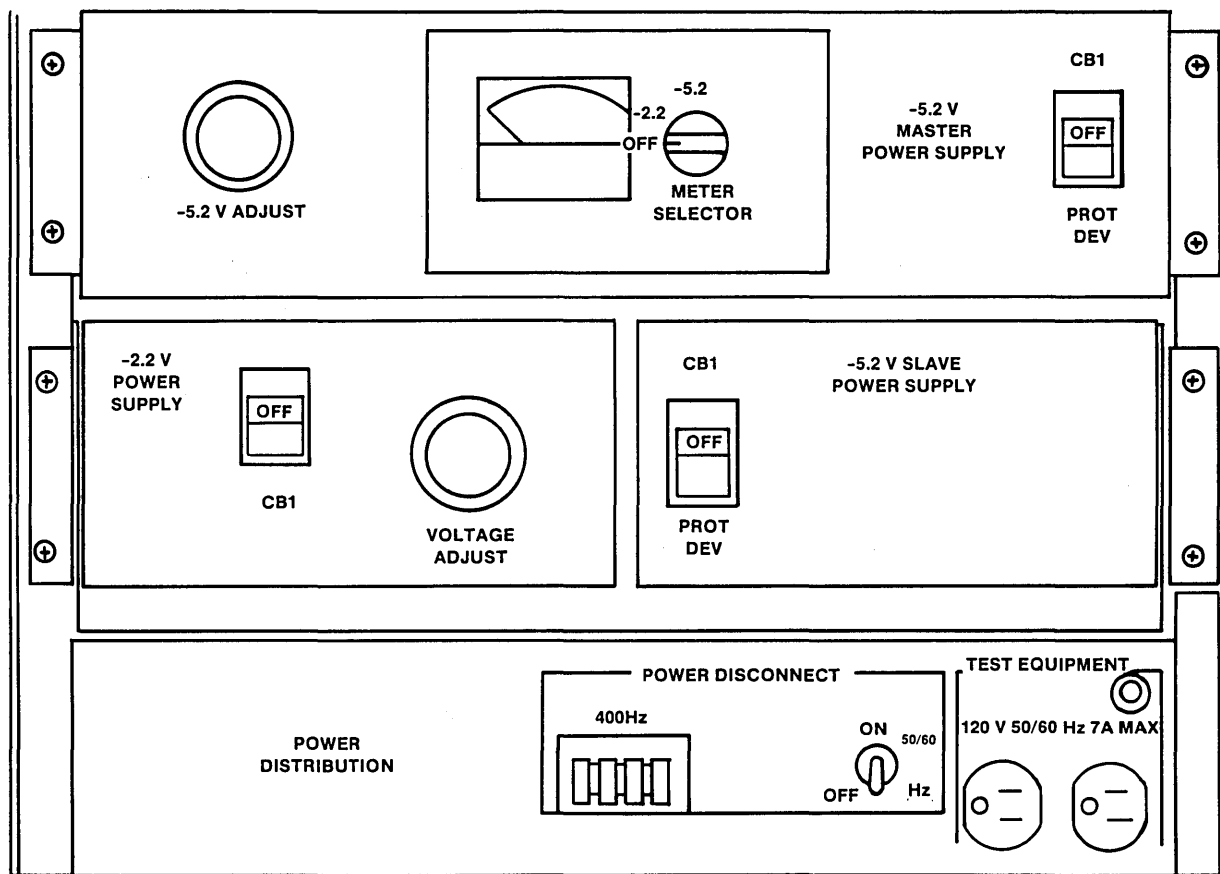


Figure 4-5. Power Supply

CYBER Fixed Module Drive
Learning Activity 4-A

Across the bottom of figure 4-5 is the power distribution box. At the lower right of the power distribution box is the test equipment outlet and its push button circuit breaker. To the left is the power disconnect area with the 60-Hz on/off toggle switch and 400-Hz circuit breaker. Inside the power distribution box are the 400-Hz and 60-Hz terminal boards, RFI filter and relays K1 and K3. The 60-Hz voltage supplies the blower. Relay K1 energizes when the air flow to the logic chassis is sufficient. K1 contacts allow K3 to energize and distribute the 400 Hz to the power supplies (see figure 4-6).

The power supplies are directly above the power distribution box. Each power supply is protected by its own circuit breaker. The voltage adjusts are located on the master -5.2 V and -2.2 V supplies. The meter is located on the -5.2 V master power supply.

NOTE

Newer controllers do not have the -5.2 V slave power supply.

The output of the -5.2 V master and slave power supplies are connected and supply voltage to the ECL 60 paks and the remote sequencing relays. The -2.2 V power supply provides voltage to the termination resistors on the ECL boards.

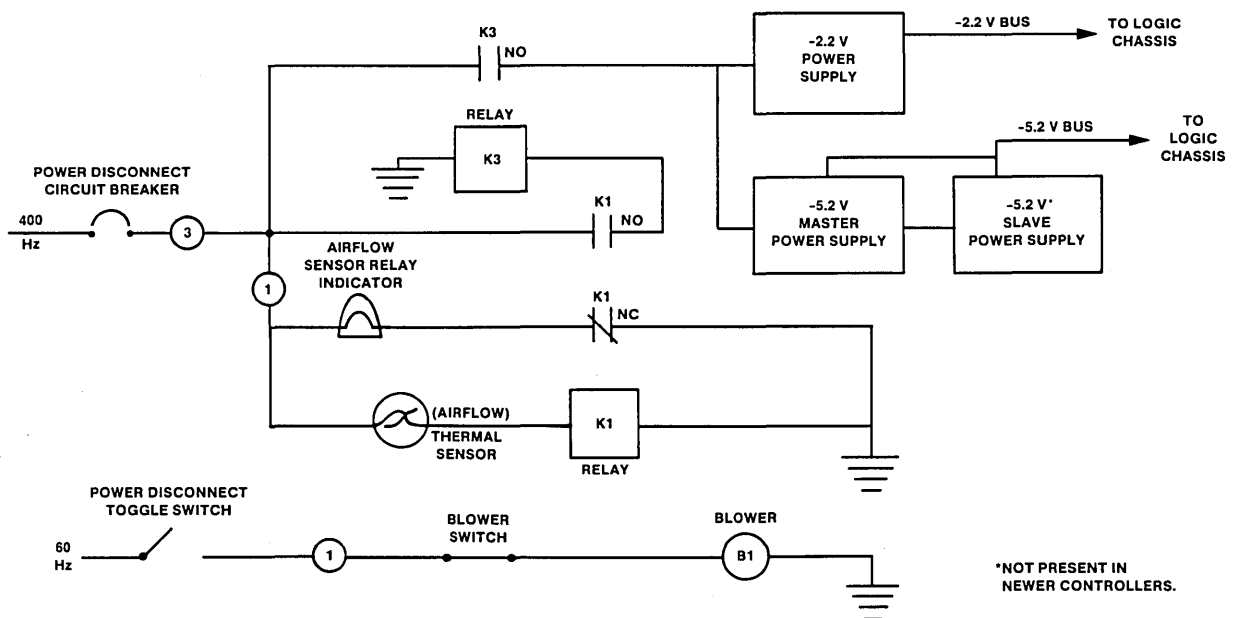


Figure 4-6. 7155 Power Distribution

CYBER Fixed Module Drive
Learning Activity 4-A

The blower is mounted above the power supplies. It supplies filtered air to cool the logic chassis directly above. Mounted on the left side of the blower assembly is the blower switch and air flow sensor relay indicator. The air flow sensor is inside the air duct (see figure 4-7).

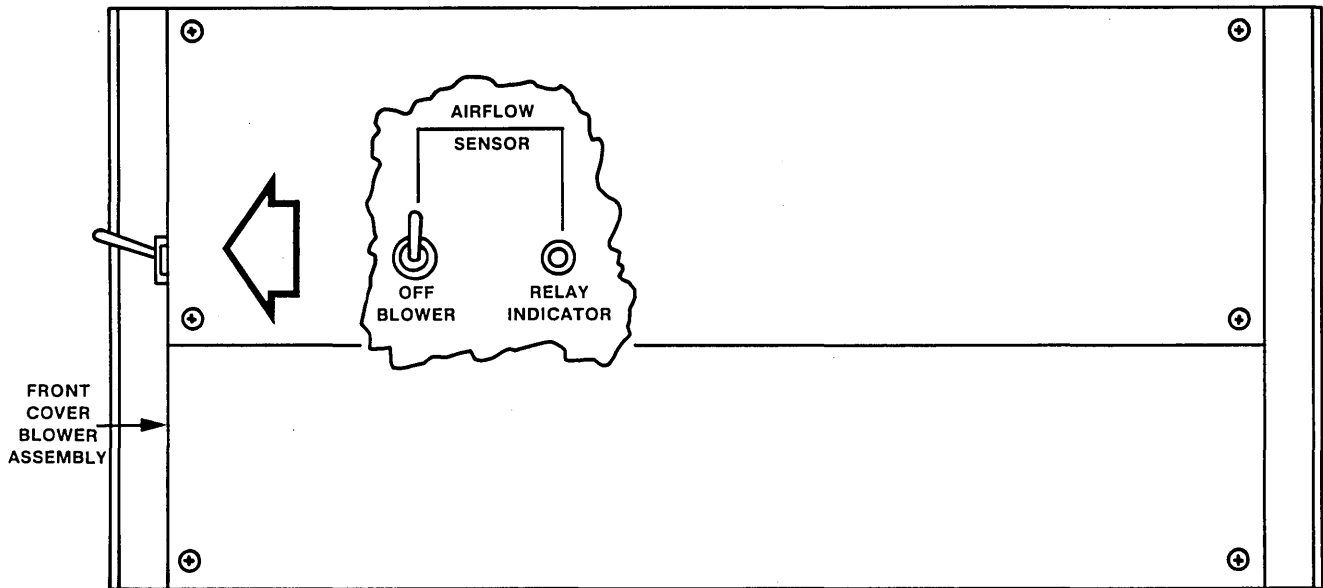


Figure 4-7. Airflow Sensor

If the temperature sensor indicates that there is not enough air flow, it causes relay K1 in the power distribution box to de-energize, which turns on the relay indicator. When K1 de-energizes, it will cause K3 to de-energize, which removes the 400 Hz from the power supplies and drops the logic voltages.

The off blower switch turns off the blower to test the air flow sensor circuit.

CYBER Fixed Module Drive
Learning Activity 4-A

The remote power sequence interface panel, at the rear of the cabinet, contains the master slave toggle switch, the sequence control in and out cable connectors, and the eight drive sequence connectors (see figure 4-8).

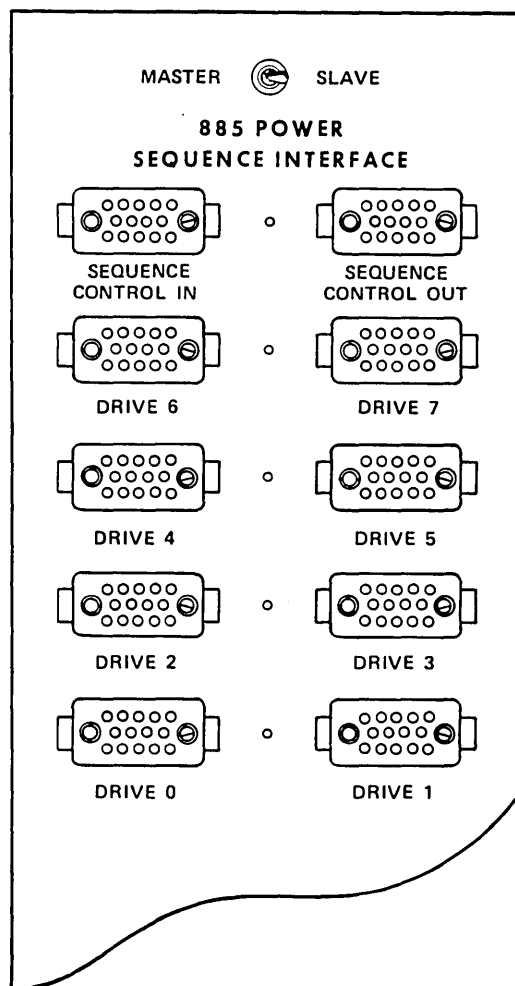


Figure 4-8. Power Sequence Interface Panel

CYBER Fixed Module Drive
Learning Activity 4-A

There are two devices to an FMD drive cabinet, so the eight connectors are sufficient for the maximum configuration of sixteen FMD devices per controller. The master slave toggle switch designates the controller as a master or slave controller in the remote power-up sequence.

The remote power-up sequence involves powering up each device in sequence before powering up the next drive. The sequence begins with powering on the controller. For a drive to power up in the remote mode, the drive's local/remote switch must be in the remote position. Any drive whose switch is in the local position will be bypassed and the following drive will be powered up.

Figure 4-9 shows a sample subsystem remote power sequencing configuration. Controller A switch is in the master position, controllers B and C are in the slave position.

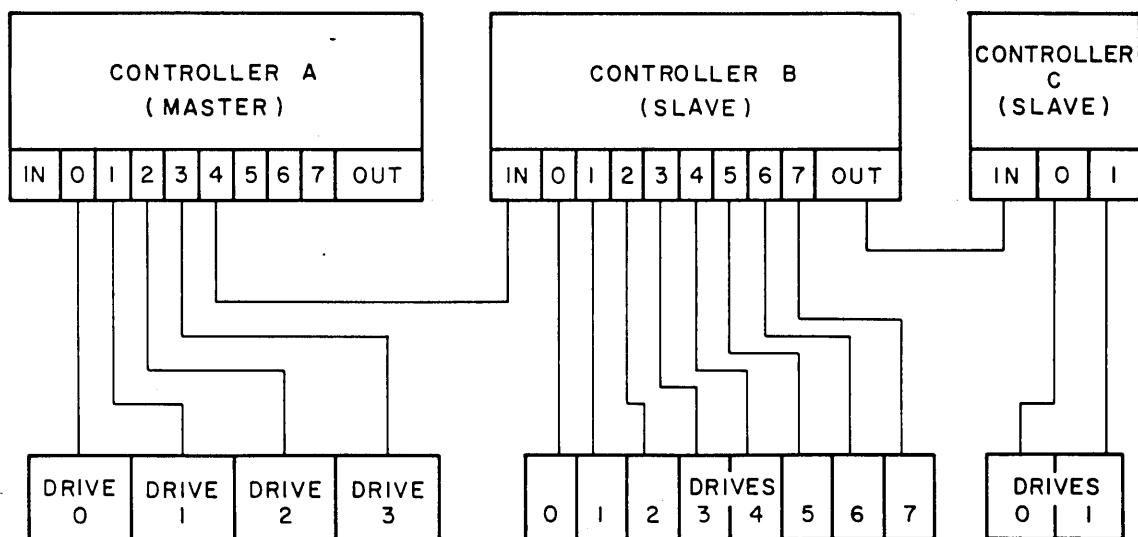


Figure 4-9. Power Sequence Cabling

CYBER Fixed Module Drive
Learning Activity 4-A

The first or only controller in an FMD subsystem must be designated as the master for the 885 power sequencing operation.

To start the sequence, controller A (master) sends the sequence signal to drive zero. Device A and B power up. Drive zero then sends the sequence signal to the controller, which passes it to drive one. The sequence repeats for each drive on the controller. The connector, after the last drive on the controller or the out connector if there are eight drives on the controller, sends the sequence signal to the in connector of the next (slave) controller. The sequence continues until the last drive on the last slave controller powers up.

Figure 4-10 shows the power sequence relays, slave master switch, and wiring to the in, out, and unit or drive cable connector.

CYBER Fixed Module Drive
Learning Activity 4-A

Relays K1 and K2 are mounted on the rear of the 885 power sequence interface panel. Relay K1 will only be used with the FV670A (844) option. The contacts of relay K1 allow the 844 remote power sequence to begin. The 844 does not have separate remote power cables but uses its existing data cables. The lines from the contacts of relay K1 go to the power sequence wiring in the 844 data cables.

Relay K2 energizes to enable the power sequence to the eight FMD units (drives) and out to the next controller. When the master slave switch is in the master position, the logic ground line is used to energize the relays. The left side of the relays is always tied to -5.2 volts. When the master slave switch is in slave position, the ground signal is supplied by the previous controller on the A line of the in connector P09.

After K2 energizes, the logic ground is supplied through the 9/11 contacts to the B line on all eight units and the out connector P010. This is the hold line to the units power supplies.

The 6/7 contacts of K2 supply the logic ground to the A line on unit 0, P01. This is the Pick In signal to the units power supply to begin a remote power-up operation. After the devices of unit 0 power up, the sequence signal will be placed on the C line from P01 to the A input to unit 1 P02. The sequence signal is called Pick Out from unit 0 line C and is called Pick In into the A input of unit one P02.

The sequence will continue, powering up the devices of unit 2 through 7 then out P010 to the in-connector of the next controller.

CYBER Fixed Module Drive
Learning Activity 4-A

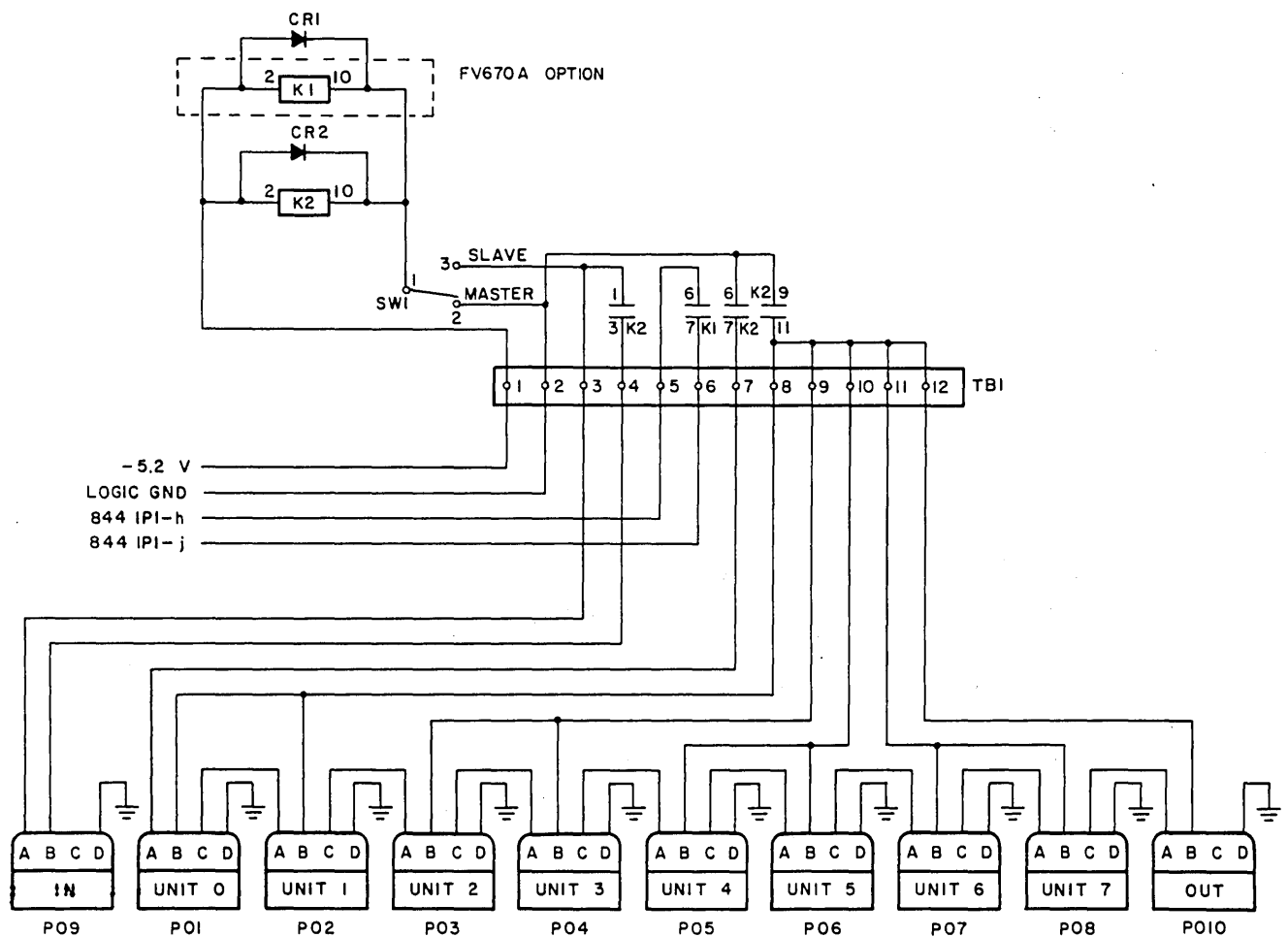


Figure 4-10. Power Sequence Wiring Diagram

LEARNING ACTIVITY 4-B. EXERCISE: CONTROLLER COMPONENTS REVIEW

This activity reviews the 7155 controller components. After completing the exercise, check your answers with those given at the end of this learning activity

OBJECTIVE

- You will be able to describe the function of the major components of the 7155 controller.

Directions: After reading each of the following statements, fill in the blank(s) with a word or words to complete the statement and make it true.

1. The 7155 controller has a switch panel located above (above/below) the logic chassis.
2. There are 4 PP channel enable/disable switches on the switch panel.
3. There are 16 885 enable/disable switches on the switch panel.
4. The Power on indicator lights when power is applied to the controller.
5. The protected/disable toggle switch is located B 13.
6. The four switches on the logic board at chassis location A08 are the parity enable switches.
7. The logic boards with LEDs are located in the A (A/B) row of logic.
8. The 7155 controller power supplies provide -2.2 volts and -5.2 volts.
9. Relay K K1, in the power distribution box, energizes when there is sufficient air flow to the logic chassis.
10. The meter for the power supplies is located on the 5.2 volt power supply.

CYBER Fixed Module Drive
Learning Activity 4-B

11. The blower operates when the 60 HZ
(60-Hz toggle switch/400-Hz CB) is turned on.
12. The logic voltages are turned off (on/off) when there is insufficient air flow.
13. The logic board at location A21 is used for channel control.
It is card type AC and its Control Data part number is 11896398.
14. The PP on the A access connects to controller, the LED on the logic board at location A8 will light.
15. The LEDs on the logic board at location 27 light when a ROM or RAM parity error is detected.
16. For an FMD to be powered up by the controller, the sequence interface cable must be connected (connected/disconnected) and the FMD's local/remote switch must be in the remote position.
17. For 885 power sequencing with only one controller in the FMD subsystem, the controller must be designated as the master controller by the master/slave toggle switch.
18. The FMD units or drives must be sequentially cabled to the power sequence connectors beginning with PO 1.
19. There are five units or drives cabled to the controller. The line to the in connector of the next slave controller must come from PO 6.
20. Power sequence relay K1 is used only if the 844 option is installed.
21. With the master slave switch in the slave position, the ground to energize relay K2 comes from the in connector P09.
22. The pick in signal to unit 0 is supplied by the 6/7 contacts of relay K K2.
23. The toggle switch on the logic board at chassis location B13 is put in the down position when running voltage margins.

CYBER Fixed Module Drive
Learning Activity 4-B

ANSWERS TO LEARNING ACTIVITY 4-B

1. above
2. four
3. FMD or 885
4. power on
5. at chassis location B13 on the front edge of the logic board.
6. parity enable
7. A
8. -5.2 volt, -2.2 volts
9. one
10. -5.2 volt
11. 60 Hz toggle switch
12. off
13. channel control, AG, 11896398
14. A08
15. parity error
16. connected, remote
17. master
18. one
19. six
20. FV670 (844)
21. slave
22. two
23. disable (down)

LEARNING ACTIVITY 4-C. TEXT READING: FUNCTIONAL ELEMENTS

This activity describes the functional elements and PP interface signals. It defines the function, parameter, data, and status words of the 7155 controller.

OBJECTIVE

- You will be able to describe the major functional elements and PP interface of the 7155 controller.

As you have studied in previous learning activities, the block diagram, figure 4-11, shows the functional elements of the 7155 controller.

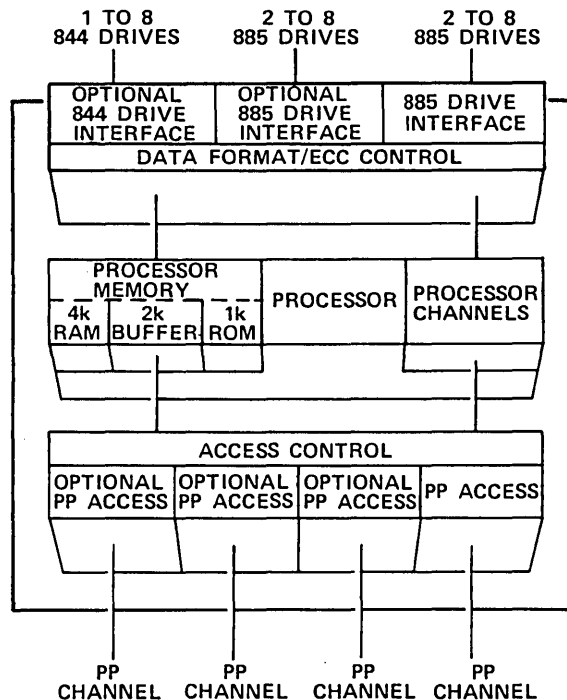


Figure 4-11. 7155 Controller Functional Elements

CYBER Fixed Module Drive Learning Activity 4-C

The PP access element represents the interface logic between the PP channel and the controller. The term PP will be used to indicate the PP and channel.

The three optional PP access elements represent the interface logic between the controller and up to three PP channels.

The access control element determines which of the four possible PP channels will be allowed to communicate with the controller on a one at a time basis.

The 885 drive interface element provides a connection between the controller and one of the eight possible FMD devices.

The optional 885 and 844 interface elements provide more connections. A maximum of sixteen FMD devices and eight 844 units may be accessed, one at a time.

The data format ECC control element directs the write and read operations and checks for data transfer errors. The checkword generator provides an error correction character (ECC) that is written on the disk at the end of the data field. The 844 ECC is 32 bits long and the 885 ECC is 48 bits long. During the read, the data and ECC character (or checkword) are both read. If the contents of the ECC circuit equals zero at the end of the read, then the logic did not detect an error. If the circuit does not equal zero, then the controller must determine whether the error is correctable. One error of eight bits or less can be corrected by the ECC logic. The data is then corrected before it is sent to the PP.

The processor area must execute a program called MA721 controlware to operate. A portion of the controlware is always present in the one-K read-only memory (ROM). The one-K-ROM is memory address 20,000 through 21,777 octal. The master clear push button on the switch panel or the PP channel master clear sends the one-K ROM to memory address 20,000 and the processor begins executing the program. The ROM controlware includes a processor instruction test, a drive release routine, and an idle loop. The program looks for PP functions, such as requests for status, and autoloading commands.

For the processor to respond to all functions, the rest of the controlware program must be loaded into the four-K-random access memory (RAM). As the controlware is loaded, additional inline diagnostics are included and executed. With the controlware in memory, the processor can respond to PP commands and control the FMD and 844 disk drives. The four-K-RAM is memory address 0 through 7777 octal.

CYBER Fixed Module Drive
Learning Activity 4-C

The process of loading the MA721 controlware into the four-K-RAM is called an autoloading operation. The controlware may be loaded from the PP or disk. The exact procedure used depends upon site operating procedures, the operating system in use, computer system configuration, and whether or not the computer system is running.

The two-K-buffer memory is used as additional storage by some controlware programs and as a data buffer when writing or reading on the disk. The two-K-RAM is memory address 10,000 through 13,777 octal.

The processor executes the controlware program from memory. The commands or functions from the PP are interpreted by the controlware program, which executes other controlware programs. The processor will then direct the controller logic to issue commands and signals to control the disk drive.

The processor communicates with the logic of the controller through the processor channels. The processor receives functions from the PP and status conditions from the disk drives and controller logic. It then transmits commands through the channels to control logic operations of the controller.

There are 15 normal input and output channels that interface the processor with the logic of the controller. There is a channel called the special CYBER channel that interfaces the processor with the access control and PP access element.

With options, a 7155 controller may have a maximum of four PP access elements. With a multiple access controller the first PP to send a function (any function) is the one that connects and reserves the controller for its use. The other PPs are locked out.

CYBER Fixed Module Drive
Learning Activity 4-C

Figure 4-12 shows the interface signals between the PP and controller.

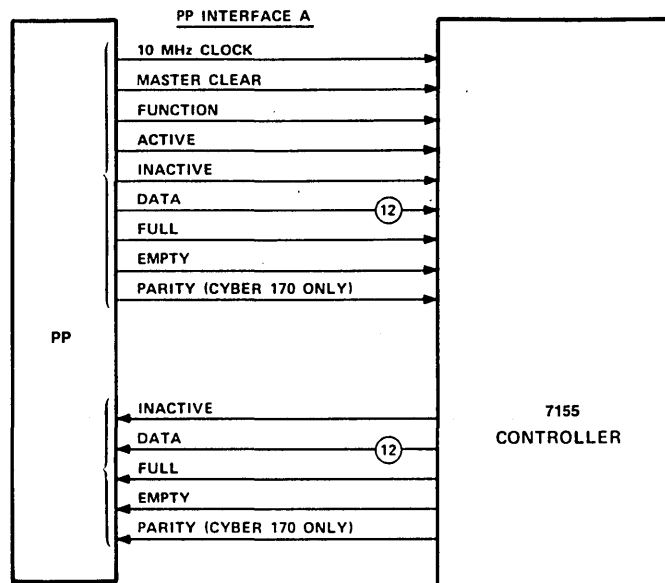


Figure 4-12. PP/7155 Controller Interface

The purpose of each signal is as follows:

- 10 MHz clock signal. The controller uses this signal to synchronize all communication with a PP.
- Active signal. The PP sends this signal to initiate or resume communication with the controller for a data transfer operation.
- Function signal. This signal identifies the accompanying 12 data signals as a function code.
- Master clear signal. The PP sends this signal to clear the controller as part of a computer system deadstart.
- Parity (CDC CYBER 170 only) signal. This signal provides odd parity for the 12 data signals it accompanies.

CYBER Fixed Module Drive
Learning Activity 4-C

- Full signal. This signal indicates to the receiver that the word formed by the 12 data signals can be accepted.
- Empty signal. This signal indicates to the transmitter that the receiver has accepted the word accompanying the last full signal.
- Inactive signal. The controller replies to a function signal (and its associated function code) with an inactive signal. An inactive signal may also be used by either the PP or the controller to terminate communication.
- Data 0-11 signals. These 12 signals carry data, function, and status between the PP and the controller.

For example, the interface signals are used in the following sequence during a write operation. Assume the disk device has been selected and the desired cylinder, head, and sector information has been processed.

The PP will send the 12-bit write function on the data lines to the controller and the function signal to identify the data as a function.

The controller will reply with an inactive signal to the PP to acknowledge the function.

The PP is now ready to output 322-12 bit data words to be written serially as 3864 bits in the data field of the sector.

The PP will send the active signal that puts the controller in the data transfer mode of operation and then output 12-bit words on the data lines to the controller. Each data word is gated into the controller by a full signal. The controller acknowledges receipt of the word and indicates it is ready for another by sending an empty signal to the PP.

The operation continues until 322 words have been transferred from the PP to the controller.

The operation may be terminated by either the PP sending an inactive signal to the controller or the controller sending an inactive signal to the PP.

CYBER Fixed Module Drive Learning Activity 4-C

After the write operation the PP requests status to determine if any error conditions occurred. The sequence of interface signals is as follows.

The PP will send the 12 bit status function on the data lines to the controller. The function signal will identify the data as a function.

The controller will reply with an inactive signal to the PP to acknowledge the function.

The PP is now ready to input the one to twenty words (depending on the status function) of status.

The PP will send the active signal which puts the controller in the data transfer mode of operation.

The controller puts the 12-bit status word(s) on the data lines to the PP. Each data (status) word is gated into the PP by a full signal. The PP acknowledges receipt of the word, and indicates it is ready for another by sending an empty signal to the controller. The operation continues until one to twenty words have been transferred from the controller to the PP.

The operation may be terminated by either the PP sending an inactive signal to the controller or the controller sending an inactive signal to the PP.

Table 4-2 lists function codes that the PP may send to the controller. The first column is the octal code of the 12-bit word. The second column is the function word itself and the remaining two columns are the number of 12 bit data words the PP must output or input.

For example, an octal code of 0005 is the write function and the PP must output the 322-12 words for the data field.

An octal code of 0012, 0013, or 0023 will request 1, 12, or 20 words of status.

Octal codes of 0001 or 0002 are seek functions. The PP must follow the function with four data words. The four words will specify the device (unit), cylinder, head, and sector address. The four data words are sometimes called parameter words because they define the seek command.

CYBER Fixed Module Drive
Learning Activity 4-C

The term seek 1:1 interlace or 2:1 interlace means the following data transfer operation will occur on consecutive (1:1) sectors or alternate (2:1) sectors.

The one parameter word following a connect (0000) function specifies to which disk device (unit) the controller will send the select signal.

The 0414 code specifies the autoload from PP function. The 14,460 words the PP outputs following the autoload function is the MA721 controlware that is loaded into the controller four-K-random access memory.

A complete description of all function codes can be found in section three of the 7155 Disk Storage Subsystem Reference Manual, publication number GF60455860.

This learning activity described the functional block diagram, PP interface signals and function codes of the 7155 controller.

CYBER Fixed Module Drive
Learning Activity 4-C

TABLE 4-2. SUBSYSTEM FUNCTIONS

Octal Code	Function	Words Output	Words Input
0000	Connect	1	
0001	Seek, 1:1 interlace	4	
0002	Seek, 2:1 interlace	4	
0004	Read		322
0005	Write	322	
0006	Write verify	322	
0007	Read checkword		
0010	Operation complete		
0011	Disable drive reserve		
0012	General status		1
0013	Detailed status		12
0014	Continue	322	322
0015	Drop seeks		
0016	Format pack	7	
0020	Drive release		
0021	Return cylinder address		1
0022	Set/clear flaw	1	
0023	Extended detailed status		20
0024	Read gap sector		322
0025	Write gap sector	322	
0026	Write verify gap sector	322	
0027	Read checkword gap sector		
0030	Read factory data		322
0031	Read utility map		322
0032	Block transfer buffer read		322
0033	Block transfer buffer write	322	
0034	Read protected sector		322
0035	Write last sector	322	
0036	Write verify last sector	322	
0037	Write protected sector	322	
0040	Read short		319
0041	Select strobe and offset	1	
0042	Clear connected access		
0043	Buffer read		322
0044	Buffer write	322	
0046	Write buffer to disk		
0047	Scan cylinder addresses		
0050	Output on processor channel	3	

TABLE 4-2 SUBSYSTEM FUNCTIONS (Contd)

Octal Code	Function	Words Output	Words Input
0051	Execute control word sequence	49	
0052	Input processor channel status		32
0053	Echo output channels		32
0054	Issue processor flag pulse	1	
0055	Enable input channel timing	1	
0056	Input timing data		2
0057	Echo one word	1	1
0060	Force instruction timeout		
0061	Autodump		12288
0062	Manipulate processor	5	
0063	Input display data		64
0064	Time difference counter		
01NN	Autoload from disk		
03NN	Disk deadstart		
0414	Autoload from PP	14460	
0720	Echo one word	1	1

CYBER Fixed Module Drive
Learning Activity 4-D

LEARNING ACTIVITY 4-D. EXERCISE: FUNCTIONAL ELEMENTS REVIEW

This activity reviews the 7155 controller functional elements.

OBJECTIVE

- You will be able to describe the major functional elements and PP interface of the 7155 controller.

After completing the exercise, check your answers with those given at the end of this learning activity.

Directions: Each of the following statements describes one of the elements listed below. After reading each statement, write the letter of the function it describes in the blank preceding it.

	<u>Statement</u>	<u>Element</u>
<u>2</u>	1. Execute controlware.	a. Access control
<u>a</u>	2. Determines PP access to be connected.	b. Buffer memory
<u>h</u>	3. Controlware is auto-loaded into.	c. Optional 885 drive interface
<u>F</u>	4. Controlware is always present.	d. Processor channels
		e. Processor
<u>g</u>	5. Generates 48 bit checkword.	f. One-K-ROM
<u>C</u>	6. Controller can have a maximum of 16 FMDs.	g. ECC control
		h. Four-K-RAM
<u>b</u>	7. Memory address 10,000 through 13,777 octal.	
<u>d</u>	8. Fifteen normal input/output and one special CYBER.	

CYBER Fixed Module Drive
Learning Activity 4-D

Directions: After reading each of the following statements, fill in the blank(s) with a word or words to complete the statement and make it true.

9. The function signal identifies the 12 data signals as a function code.
10. The full signal indicates the 12 data signals can be accepted as a data, parameter, or status word.
11. The active signal is sent to the controller before a data transfer operation begins.
12. An octal function code of 0004 indicates that 322 12-bit words will be read from the disk.
13. To request the one word of general status, the PP sends the octal function code of 12.
14. A request for extended detailed status will send 20 12-bit words to the PP.
15. any function code will connect a PP channel to the 7155 controller.

CYBER Fixed Module Drive
Learning Activity 4-D

ANSWERS FOR LEARNING ACTIVITY 4-D

1. e
2. a
3. h
4. f
5. g
6. c
7. b
8. d
9. function
10. full
11. active
12. three hundred twenty-two
13. 0012
14. twenty
15. Any

LEARNING ACTIVITY 4-E. TEXT READING: STATUS WORDS

This activity describes the general and detailed status words for the 885 FMD and 844 disk drives on the 7155 controller.

OBJECTIVE

- You will be able to identify the status words and describe the function of each word.

One to twenty words of status are available to the PP. An octal function code of 0012 requests one word of status called the general status word.

CYBER Fixed Module Drive
Learning Activity 4-E

Table 4-3 describes the purpose of each bit of the 12-bit general status word. All bits of the general status word equal to zero indicates a normal function completion.

TABLE 4-3. GENERAL STATUS

Bit	Definition
11	Abnormal termination. Preceding function terminated abnormally. General status bits 8 and 9 indicate whether recovery is possible. Detailed status shows cause of abnormal termination.
10	Multiple-access controller reserved. Controller is reserved to another PP channel. All other status bits are meaningless.
9	Nonrecoverable error. Controller detected error from which no recovery is possible. Detailed status identifies error.
8	Recovery in process. Controller is ready to attempt error recovery in response to 0014 (continue) function.
7	Checkword error. Controller detected checkword error in address field or data field of sector. Detailed status word 2, bits 8 through 11, provides error analysis.
6	Correctable address error. Controller detected correctable read address checkword error. 0014 (continue) function enables data to be processed on subsequent disk revolution.
5	Unused.
4	Drive malfunction. Drive-related error occurred. Detailed status reflects drive status at time of malfunction.
3	Drive reserved. Requested drive is reserved by other controller.
2	Autoload error. Controlware loaded is not compatible with controller.
1	Busy. Controller and/or requested drive are busy.
0	Unused.

CYBER Fixed Module Drive
Learning Activity 4-E

An octal code of 0013 requests 12 words of detailed status. An octal code of 0023 requests 20 words of extended detailed status. The extended detailed status includes the twelve words of detailed status plus eight additional words. It is not normal for all bits of the detailed status words to be zero. Each word and bit must be examined carefully to determine normal or abnormal conditions.

Table 4-4 shows the first four words of detailed status and lists the purpose of each bit. Notice some bits are only applicable when operating with 885 FMDs on the 7155 controller.

TABLE 4-4. DETAILED STATUS

	11	10	9	8	7	6	5	4	3	2	1	0
WORD 1	STROBE/OFFSET RETRY COUNT								ADDRESS ERROR	CYLINDER NUMBER ERROR	TRACK NUMBER ERROR	SECTOR NUMBER ERROR
2	ADDRESS CHECKWORD ERROR	NONCORRECT-TABLE ADDRESS CHECKWORD ERROR	DATA CHECKWORD ERROR	NONCORRECT-TABLE DATA CHECKWORD ERROR	844: NOT APPLICABLE							
				885: HDA SEQUENCE COMPLETE	885: SEQUENCE LATCH 4	885: SEQUENCE LATCH 2	885: SEQUENCE LATCH 1	885: SEQUENCE CHECK LATCH	885: INHIBIT HDA CYCLE	885: AIR SWITCH LATCH	885: MOTOR AT SPEED SWITCH LATCH	
3	CURRENT FUNCTION BITS 7:0								ILLEGAL PARAMETER	ILLEGAL NUMBER OF PARAMETERS	ERROR RATE THRESHOLD EXCEEDED	
4	1	7155 SUBSYSTEM CONTROLWARE	CONTROLWARE REVISION NUMBER					DRIVE NUMBER BITS 5:0				

CYBER Fixed Module Drive Learning Activity 4-E

Table 4-5 shows words 5 through 12 of detailed status as they apply to 885 FMDs on the 7155 controller.

TABLE 4-5. 885 DETAILED STATUS

	11	10	9	8	7	6	5	4	3	2	1	0		
WORD 5	TRACK FLAW	FACTORY FLAW MAP FLAW					CYLINDER NUMBER BITS 9-4							
6	CYLINDER NUMBER BITS 3-0					TRACK NUMBER BITS 7-0								
7	SECTOR NUMBER BITS 7-0								READY AND SAFE	SYSTEM MAINTENANCE MODE	DRIVE NUMBER BITS 6 AND 7			
8	DRIVE NUMBER BITS 5-0						FIXED HEADS INSTALLED	WRITE ENABLE	ONLINE	AIR SWITCH	START SWITCH ON	MOTOR AT SPEED	885 DRIVE ONLY	
9	INDEX	SECTOR MARK/ON SECTOR	ON CYLINDER	SELECTED AND RESERVED	READY AND SAFE	ON SECTOR	STATUS VALID	STATUS PARITY ERROR	SEEK TIMEOUT ERROR	SEEK OVERSHOOT ERROR	SERVO OFF TRACK	REZERO MODE LATCH		
10	SERVO LATCH	LINEAR MODE LATCH	CONTROL LATCH	WAIT LATCH	LAST SEEK FORWARD	GUARD BAND PATTERN CROSSED	TARGET VELOCITY	TRACK CROSSING			ODD TRACK	ON CYLINDER		
11	CAPABLE ENABLE ERROR	WRITE OVERRUN	MULTIPLE HEAD ERROR	WRITE CURRENT ERROR	WRITE TRANSITION ERROR	CONTROL ERROR	INDEX CHECK	HEAD SHORT	WRITE + READ + NO CONTROL SELECT ACTIVE	WRITE WHILE IN OFFSET				
12	EARLY STROBE	LATE STROBE	FORWARD OFFSET	REVERSE OFFSET		SECTOR COMPARE ERROR	DRIVE ERROR		READ/ WRITE ERROR		ACCESS CHECK			
	11	10	9	8	7	6	5	4	3	2	1	0		

Table 4-6 shows words five through twelve of detailed status as they apply to 844s on the 7155 controller.

CYBER Fixed Module Drive
Learning Activity 4-E

TABLE 4-6. 844 DETAILED STATUS

	11	10	9	8	7	6	5	4	3	2	1	0	
5	CYLINDER NUMBER BITS 8-0									TRACK NUMBER BITS 4-2			
6	TRACK NUMBER BITS 1, 0		SECTOR NUMBER BITS 4-0				SECTOR FLAW	TRACK FLAW	FACTORY MFG DATA/FLAW MAP FLAG	UTILITY FLAW MAP FLAG	CYLINDER NUMBER BIT 9		
7													844 DRIVE ONLY
8													
9	SECTOR ALERT	SEEK ERROR	BUSY	SELECTED	READY	ONLINE	844-4X DRIVE			END OF CYLINDER	SEEK ERROR; END OF TRAVEL	INDEX MARK	
10	ON CYLINDER	SEEK ERROR; NOT ON CYLINDER	PACK UNSAFE	SECTOR MARK	SEEK ERROR	-VOLT	+VOLT	CURRENT	WRITE READ	WRITE + READ + NOT ON CYLINDER	AC WRITE FAULT		
11	LOGIC TEMPERATURE NORMAL	SPINDLE MOTOR ON	REMOTE POWER SEQUENCE	START SWITCH ON	BRUSH CYCLE	HEADS LOADED	PHYSICAL ENABLE	PACK ON					
12													
	11	10	9	8	7	6	5	4	3	2	1	0	

Table 4-7 shows the eight additional words of extended detailed status. Notice in words 13, 14, and 15 bits 0 through 7 apply only to an 885 FMD error. A read/write error in either an 844 or 885 FMD will use bits 0 through 8 of word 13 and all 12 bits of words 14 and 15.

TABLE 4-7. EXTENDED DETAILED STATUS

	11	10	9	8	7	6	5	4	3	2	1	0	
WORD 13	BUFFER TO DISK ERROR	ACCESS CONNECTED BEFORE GENERAL STATUS	DRIVE RE-SERVED BEFORE SEEK/CONNECT		885 CONNECT/SEEK ERROR: DRIVE COMMAND CAUSING ERROR								
					READ/WRITE ERROR: WORD ADDRESS OF CORRECTABLE READ DATA								
	14					885 CONNECT/SEEK ERROR: DRIVE UNSELECTED STATUS FOR COMMAND IN WORD 13							
				READ/WRITE ERROR: CORRECTION VECTOR WORD 1									
15					885 CONNECT/SEEK ERROR: DRIVE ECHO STATUS FOR COMMAND IN WORD 13								
	READ/WRITE ERROR: CORRECTION VECTOR WORD 2												
16	LOST DRIVE CLOCK	UNUSED, BUT RESERVED			ECC RESIDUE NONZERO	DATA PARITY ERROR	PROCESSOR INSTRUCTION TIMEOUT	LOST CONTROL WORD	UP/DOWN COUNT NONZERO	PACK UNSAFE OR NOT READY AND SAFE	BUFFER OUTPUT REGISTER PARITY ERROR	WRITE VERIFY ERROR	0023- EXTENDED DETAILED STATUS FUNCTION ONLY
17	SYNC BYTE SEARCH IN PROGRESS	SECTOR LENGTH VIOLATION	LOST DATA	SYNC BYTE MISCOMPARE	CHECKWORD ERROR CORRECTION IN PROGRESS	BUFFER OUTPUT REGISTER FULL	BUFFER INPUT REGISTER FULL	CHANNEL RESERVED	DEADMAN TIMEOUT	CHANNEL INACTIVE	DATA FIELD ERROR	ADDRESS FIELD ERROR	
18	ACCESS D CONNECTED	ACCESS C CONNECTED	ACCESS B CONNECTED	ACCESS A CONNECTED	LAST FUNCTION BITS 7:0								
19					SECOND TO LAST FUNCTION BITS 7:0						THIRD TO LAST FUNCTION BITS 7:4		
20	THIRD TO LAST FUNCTION BITS 3:0				FOURTH TO LAST FUNCTION BITS 7:0								
	11	10	9	8	7	6	5	4	3	2	1	0	

CYBER Fixed Module Drive
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TABLE 4-8. EXTENDED DETAILED STATUS REVISION 4

	11	10	9	8	7	6	5	4	3	2	1	0	
WORD 18	ACCESS D CONNECTED	ACCESS C CONNECTED	ACCESS B CONNECTED	ACCESS A CONNECTED	MA722 CONTROL- WARE LOADED	UNUSED							0023- EXTENDED DETAILED STATUS FUNCTION ONLY 885 CONTROLWARE REVISION 4 AND UP
19	UNUSED												
20	UNUSED			LARGE SECTOR MODE	CONTROLLER NUMBER BITS 0-7								

Table 4-8 shows the changes to the last three words of extended detailed status for controllers using revision 4 and up of the MA721 controlware.

A complete description of all status words can be found in section 3 of the 7155 Disk Storage Subsystem Reference Manual, publication number 60455860.

This learning activity listed the general and detailed status words of the 7155 controller.

LEARNING ACTIVITY 4-F. EXERCISE: STATUS WORDS REVIEW

This activity reviews the 7155 controller status words.

OBJECTIVE

- You will be able to identify the status words and describe the function of each word.

After completing the exercise, check your answers with those given at the end of this learning activity.

Directions: After reading each of the following statements, fill in the blank(s) with a word or words to complete the statement and make it true.

1. A general status of 2000 octal indicates other access received.
2. The controller detected a data field checkword error. Bit 7 of the general status word will be set.
3. Word 2 of detailed status is 0400 octal, this indicates noncorrectable data checkword error.
4. Detailed status words 5 through 12 are either for an 885 FMD or an 844 disk unit.
5. The FMD cylinder number is contained in detail status words 5 6.
6. The FMD drive number is contained in detailed status words 7, 8.
7. Detail status words 13 through 20 are requested by a PP function code of 23.
8. The PP on the A access is connected to the 7155 controller. Bit 8 of detailed status word 18 will be set.
9. A general status of 5000 octal indicates abnormal termination and nonrecoverable error.
10. The FMD that the select signal is sent to is reserved by the other controller. Bit 3 of the general status word will be set.

CYBER Fixed Module Drive
Learning Activity 4-5

ANSWERS TO LEARNING ACTIVITY 4F

1. multiple-access controller reserved
2. seven, other bits may also be set
3. data checkword error
4. five, twelve
5. five and six
6. seven and eight
7. 0023 extended detailed status
8. eight
9. abnormal termination, non-recoverable error
10. three

LEARNING ACTIVITY 4-G. AUDIOTAPE: 7155 BLOCK DIAGRAM

This activity describes the 7155 controller block diagram.

OBJECTIVE

- You will be able to list the logic boards of the 7155 controller block diagram and describe the function of each.

Figures 4-13 through 4-18 contain the 7155 controller block diagram. Notice that different areas on each page are highlighted. As you listen to the tape, the highlighted areas in each figure will be described. You may stop the tape at any time to take notes or go over some topics again.

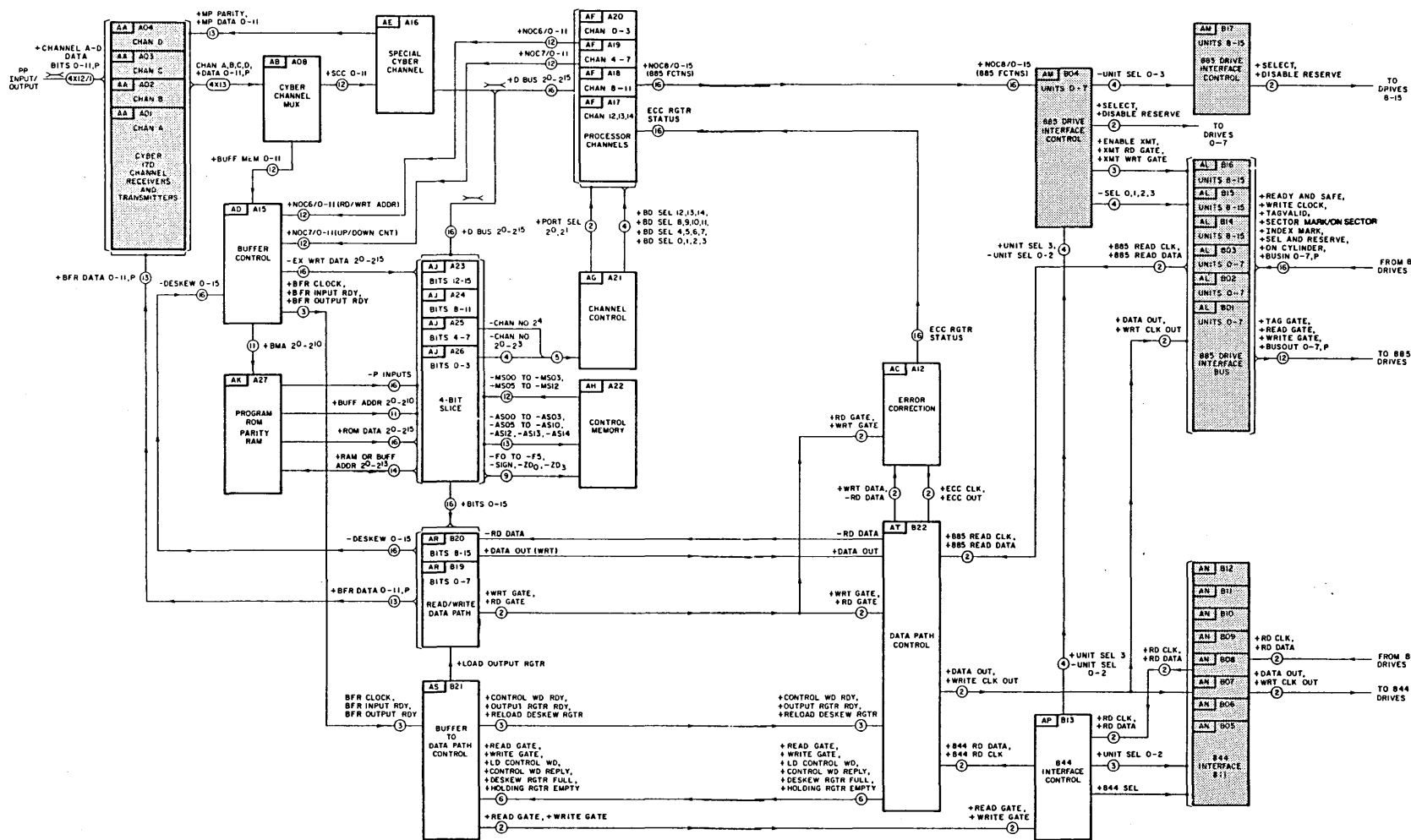
Load the audiotape 7155 Block Diagram (75445257) into your cassette player and turn to the block diagram in figure 4-13.

NOTE

The script of this audiotape is in appendix D.

STUDENT NOTES

Figure 4-13. 7155 Controller Block Diagram Interface



A



D



B

A

Figure 4-16. 7155 Controller Block Diagram Function and Status

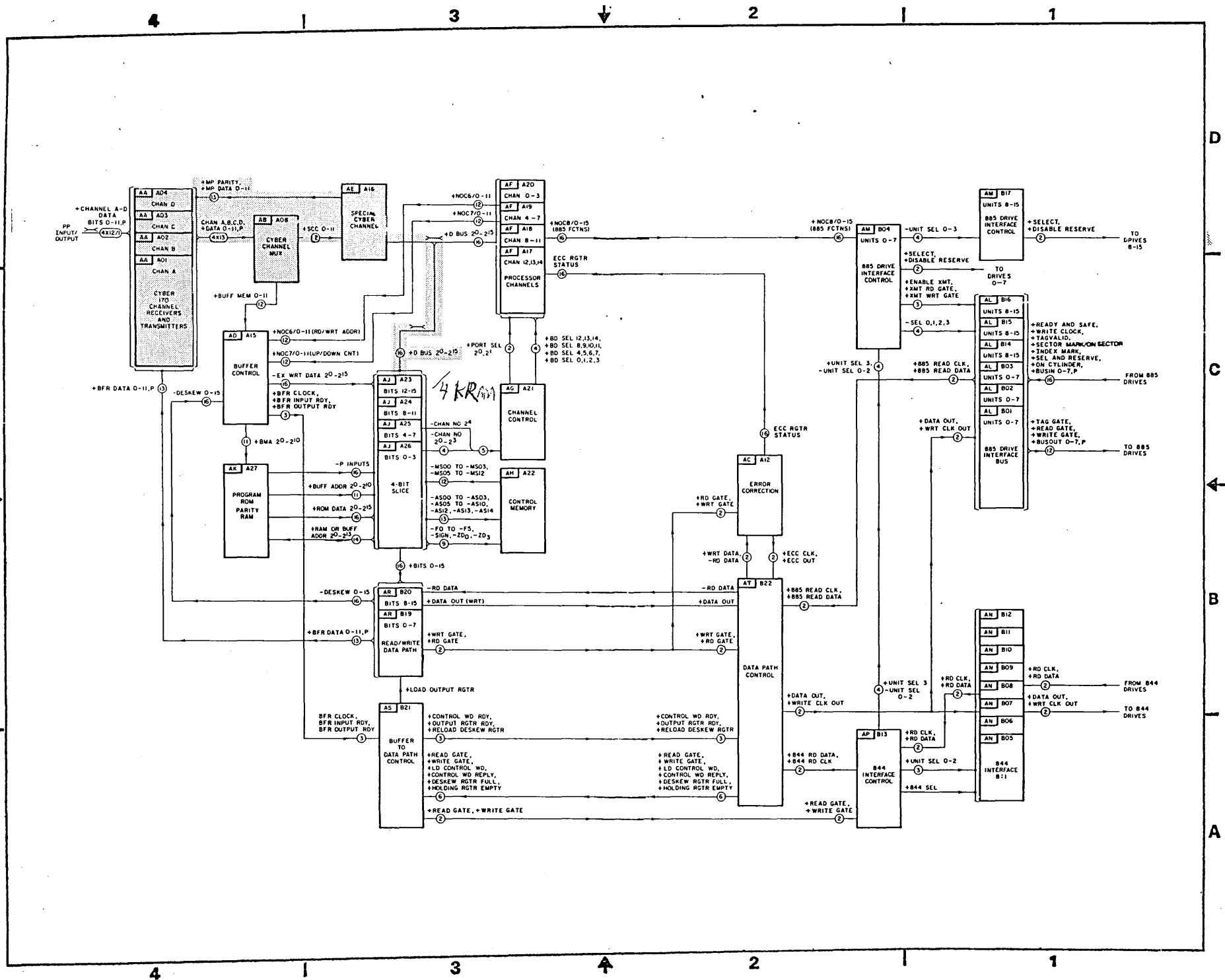
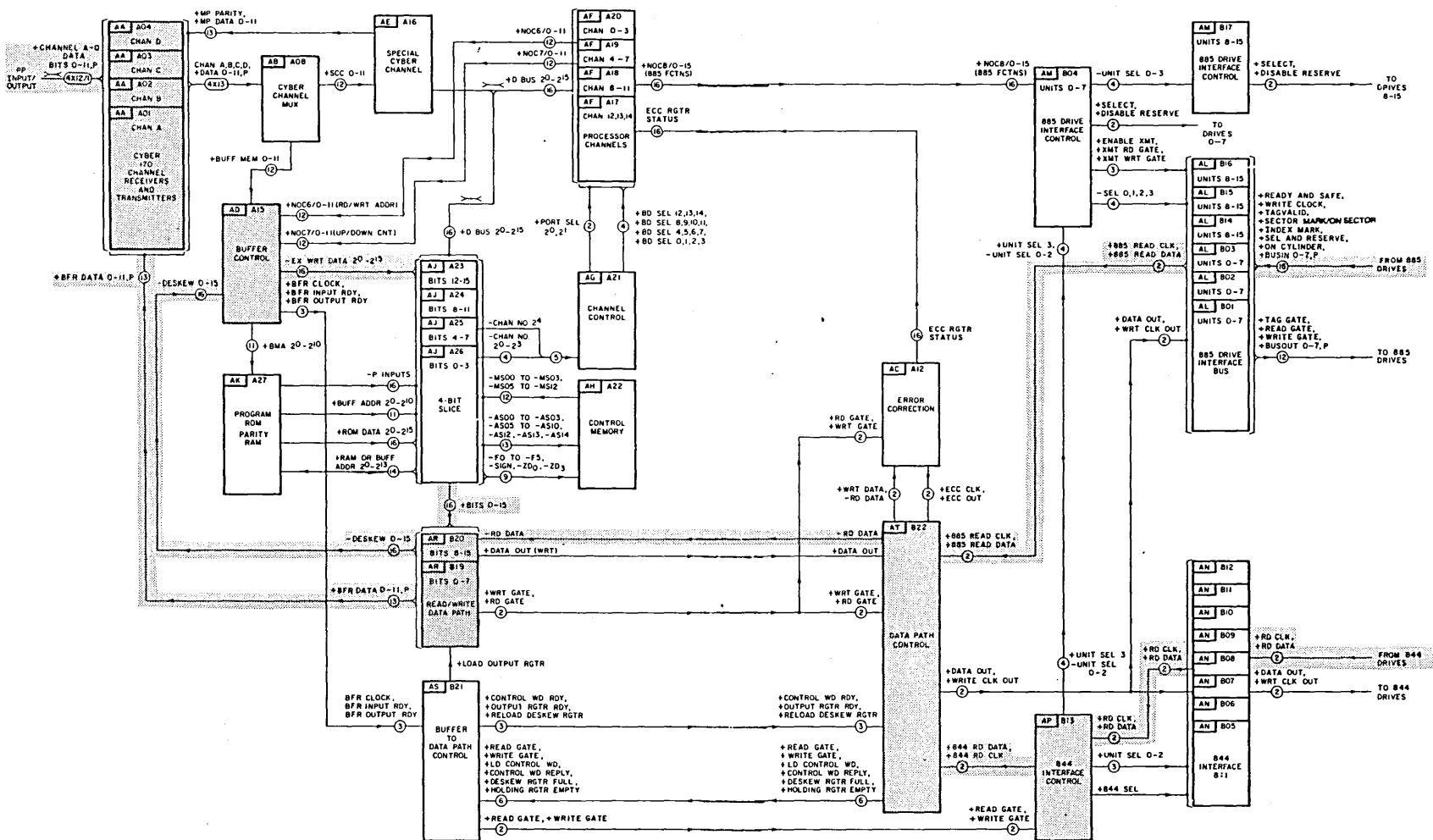


Figure 4-18. 7155 Controller Block Diagram Read



CYBER Fixed Module Drive
Learning Activity 4-H

LEARNING ACTIVITY 4-H. EXERCISE: 7155 BLOCK DIAGRAM REVIEW

This activity reviews the 7155 controller block diagram.

OBJECTIVE

- You will be able to list the logic boards of the 7155 controller block diagram and describe the function of each.

After completing the exercise, check your answers with those given at the end of this learning activity.

Directions: After reading each of the following statements, fill in the blanks(s) with a word or words to complete the statement and make it true.

1. The receivers and transmitters for PP channel B are on the AA type of logic board at location A02.
2. The FMD device select signal for device 9 is sent by the _____ type of logic board at location _____.
3. The logic boards at locations B05 through B12 are present only with the 844 option.
4. A PP receiver transmitter board must always be present at location A01 for proper signal termination.
5. The logic boards at locations B14 through B17 are present only with the 285-8-15 option.
6. The two-K-buffer memory is on the logic boards at locations A23 through A26.
7. The processor has 16 normal input and output channels on the logic board at locations A17 through A20.
8. The microcode ROM is on the logic board at location A22.
9. The microcode ROM has 60 bit words in 256 memory locations.
10. The board at location A-27 contains the one K program ROM.

CYBER Fixed Module Drive
Learning Activity 4-H

11. The four-K-RAM is a 16 bit word memory and is loaded with the MA 221 controlware.
12. The microcode control memory has a parity error indicator on the logic board at location A22.
13. The octal code of the normal input/output channel selected by the processor is displayed by LEDs on the logic board at location A21.
14. The processor uses the D bus to read the input channels and to set bits in the output channels.
15. The logic board at location A16 contains the special CDC CYBER channel, also referred to as channel number _____.
16. The special CDC CYBER channel is a bidirectional channel between the PP and the processor.
17. The LED that lights with an autoloader function is on the logic board entitled Cyber Channel map.
18. A Deadman timeout condition occurs and lights an LED on the logic board at location A08 when the PP activates the controller but sends no data for more than 7.5 seconds.
19. The up/down counter on the logic board at location A15 is loaded by the processor normal output channel NOC 07.
20. The logic board at location A12 is entitled AC error correction and has a 48 bit checkword generator circuit.
21. A 48 bit checkword is used with the 885 and a 32-bit checkword is used with 844.
22. The shift register on the logic boards at locations B19 and B20 is used to change data from parallel to serial during a write operation.
23. The shift register on the logic boards entitled read/write data path is used to change data from serial to parallel during a read operation.
24. The AP type of logic board entitled 844 interface control sends the 844 select signal and the 885 unit select signal to the AM type of logic board.

CYBER Fixed Module Drive
Learning Activity 4-H

25. The serial write data passes through the board at location B22 on its way to the error correction board and the drive interface boards.
26. The write data words from the PP pass through AA type logic board to the AB type logic board, to the AB type logic board to the two K-RAM buffer memory on the AJ type logic board.
27. The read data from the read/write data path logic board passes through the logic board entitled Buffer control to the 4-bit slice processor logic board.
28. The read data from the 4-bit slice processor passes through the logic boards entitled read/write data path to the CDC CYBER 170 channel receivers and transmitters logic board.
29. The general status word passes from the 4-bit slice processor on the D bus to the special CDC CYBER channel.
30. The PP function word passes through the AA type logic board, through the AB type logic board, through the AE type logic board to the AJ type logic board.

CYBER Fixed Module Drive
Learning Activity 4-H

The answers to this learning activity are on the following page.

CYBER Fixed Module Drive
Learning Activity 4-H

ANSWERS TO LEARNING ACTIVITY 4-H

- | | |
|--|---|
| 1. AA, A02 | 16. processor |
| 2. AM, B17 | 17. CYBER channel mux |
| 3. 844 (FV670) | 18. deadman, 4.5 ± 1.5 seconds |
| 4. A01 | 19. A15, seven |
| 5. eight additional FMD
devices (FV671) | 20. error correction,
forty-eight |
| 6. A23 through A26 | 21. forty-eight, 844s |
| 7. fifteen, A17 through A20 | 22. B19 and B20, serial |
| 8. A22 | 23. serial, read |
| 9. sixty, two hundred
fifty-six | 24. 844 interface control,
885 (FMD) |
| 10. one | 25. B22 |
| 11. sixteen, 721 | 26. AB, AD, AJ |
| 12. A22 | 27. buffer control |
| 13. A21 | 28. read/write data path |
| 14. D bus | 29. D bus |
| 15. A16, sixteen | 30. AB, AE |

POST TEST

When you have completed the learning activities assigned for module 4, sign on to the PLATO terminal and take the module 4 test.

You may use your student manual and your reference manuals during the test. Be sure to take them with you to the PLATO terminal.

Depending on the results of the test, you will be told to review some of the activities in this module or to go on to module 5.

COMMENT SHEET

MANUAL TITLE CYBER Fixed Module Drive Subsystem Fault Isolation VOL. 1

PUBLICATION NO. 75445356 REVISION F Prod. No. R0801

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